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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%. 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS. 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.												REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
												1	0006782329	ENGINEERING RELEASED	2016-08-10
DESIGN: X502/MLB_CATZ															
LAST CHANGE: Tue Aug 9 17:02:57 2016															
LAST_MODIFICATION=Tue Aug 9 17:03:06 2016															
LAST_MODIFICATION=Tue Aug 9 17:03:06 2016															
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60 78 PMIC IC & Power Control															
61 79 PMIC VCCPCH VCCIO 1.8V															
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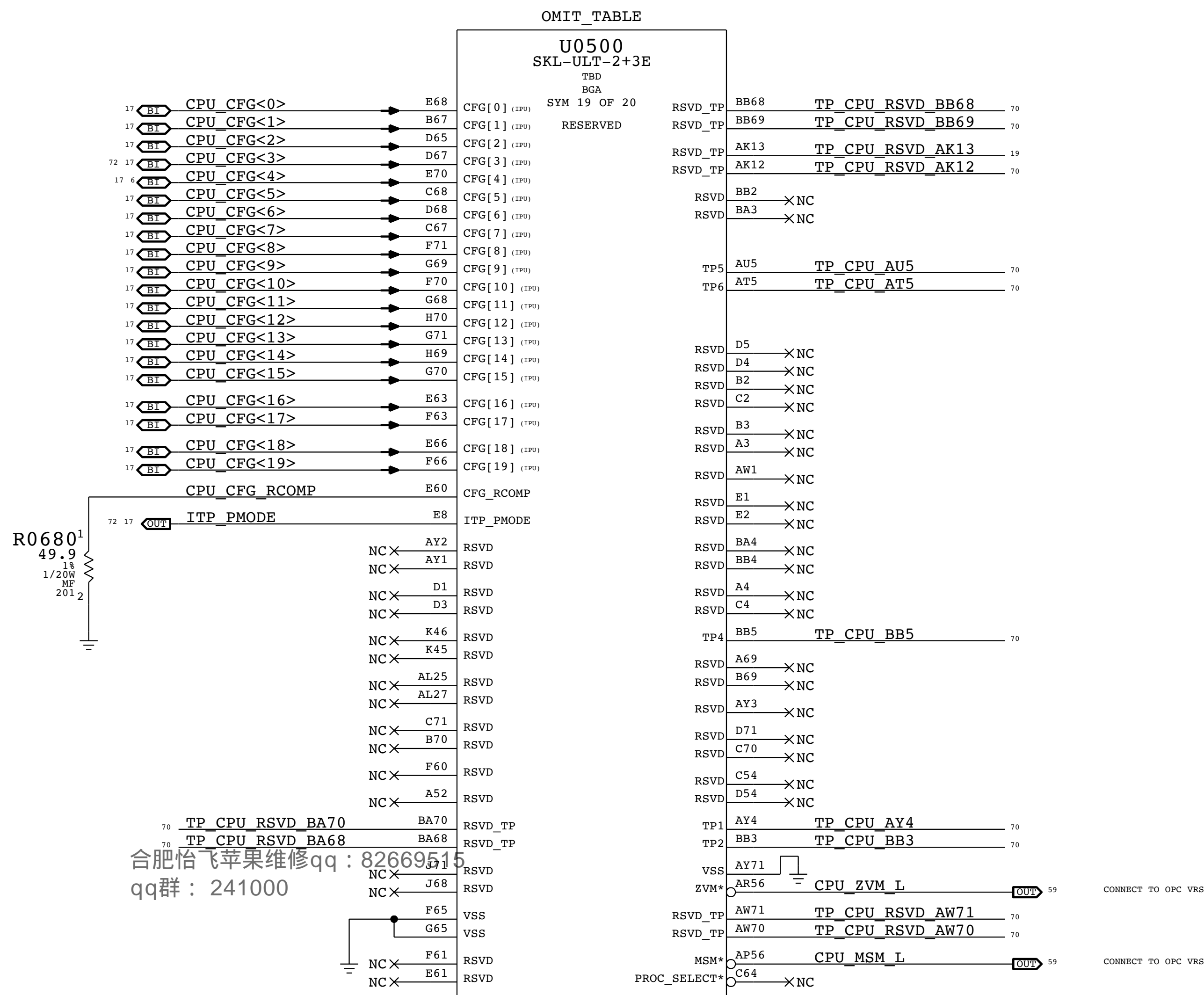
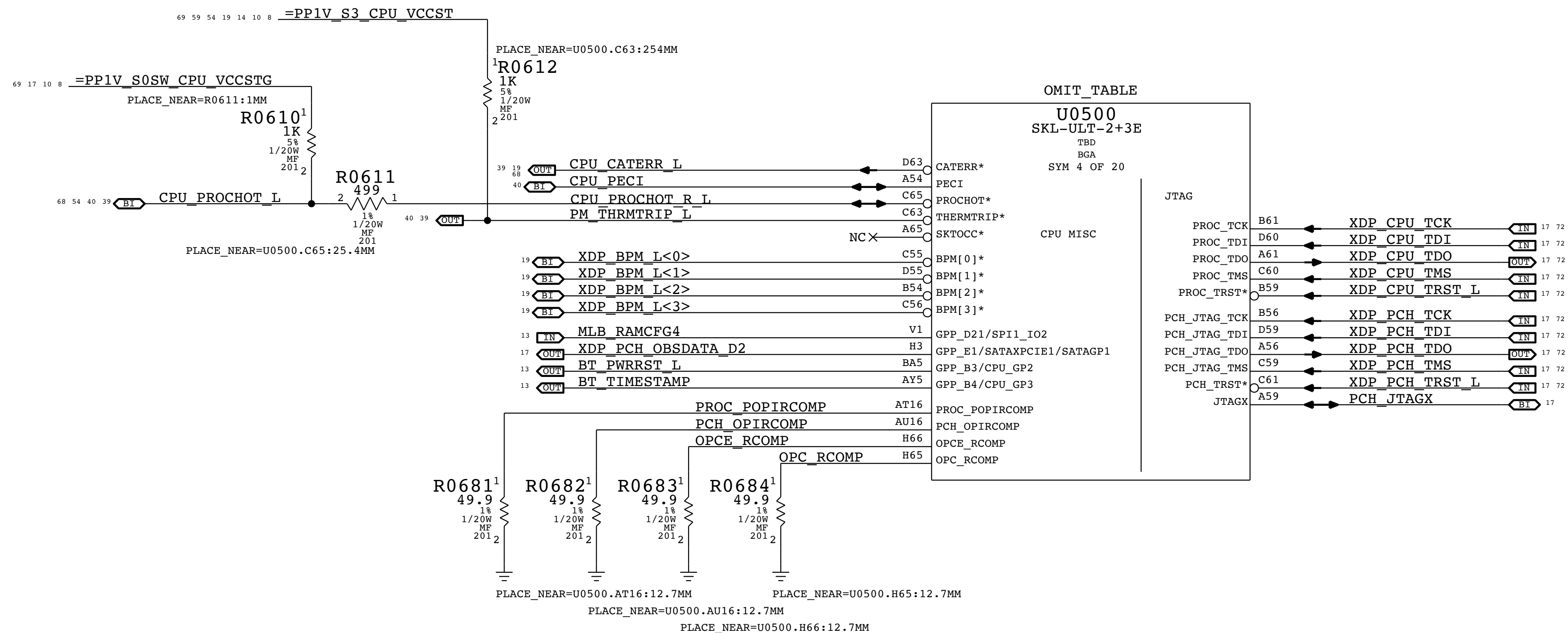
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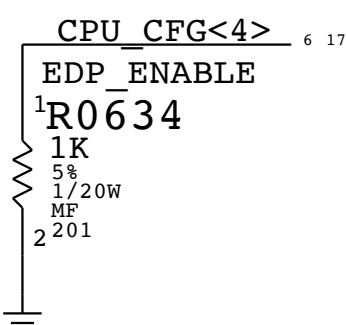







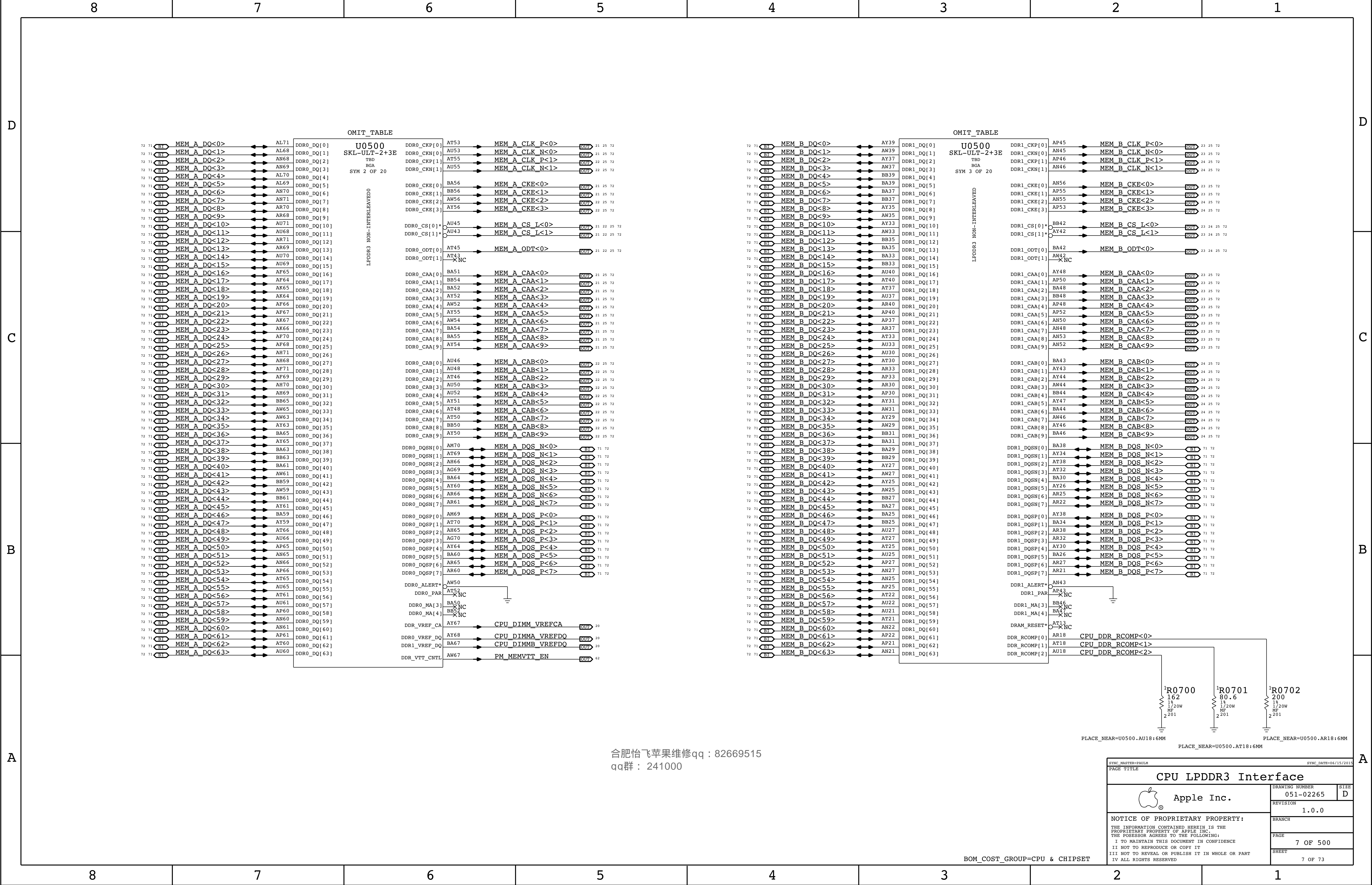


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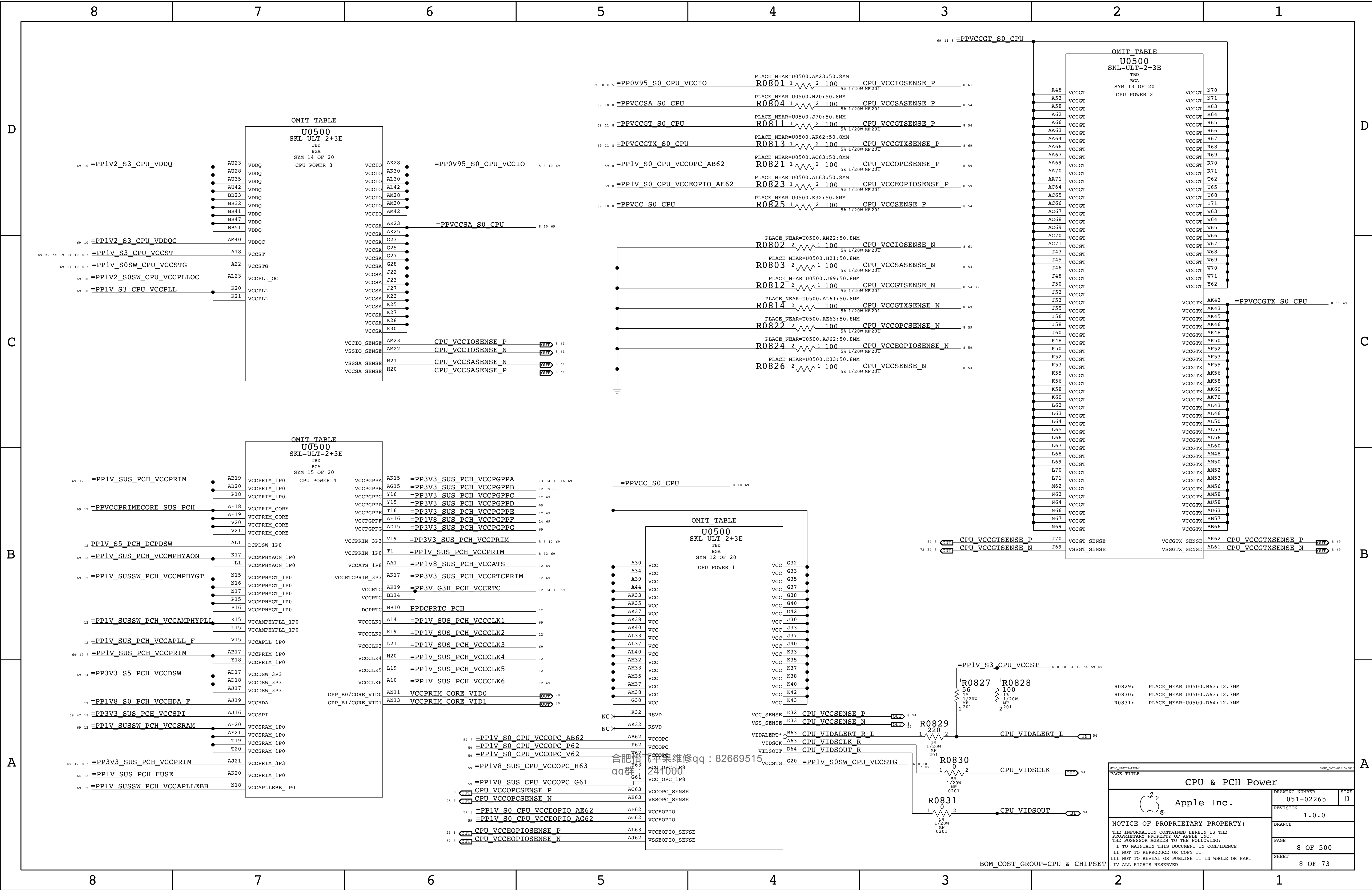
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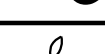




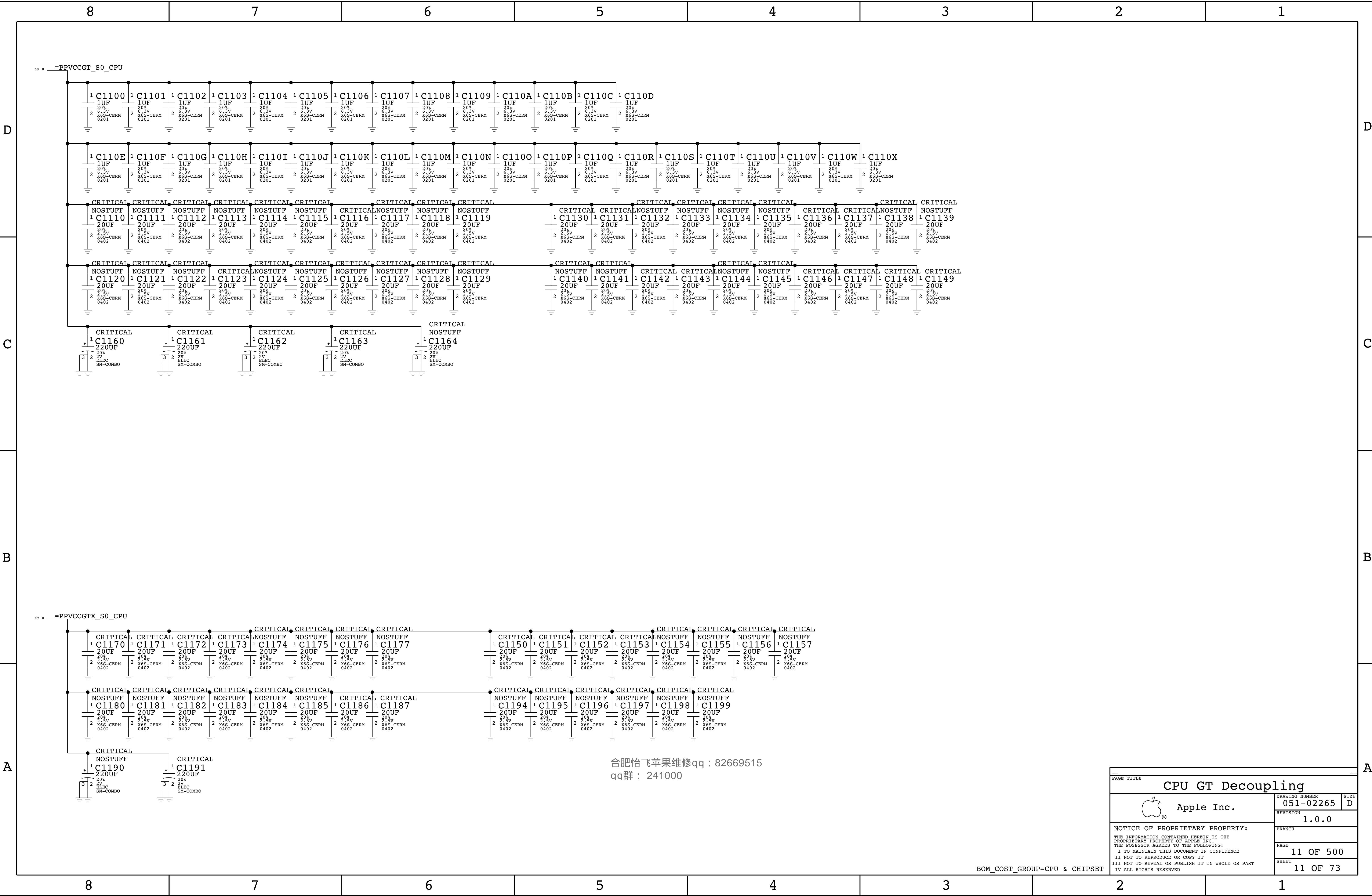





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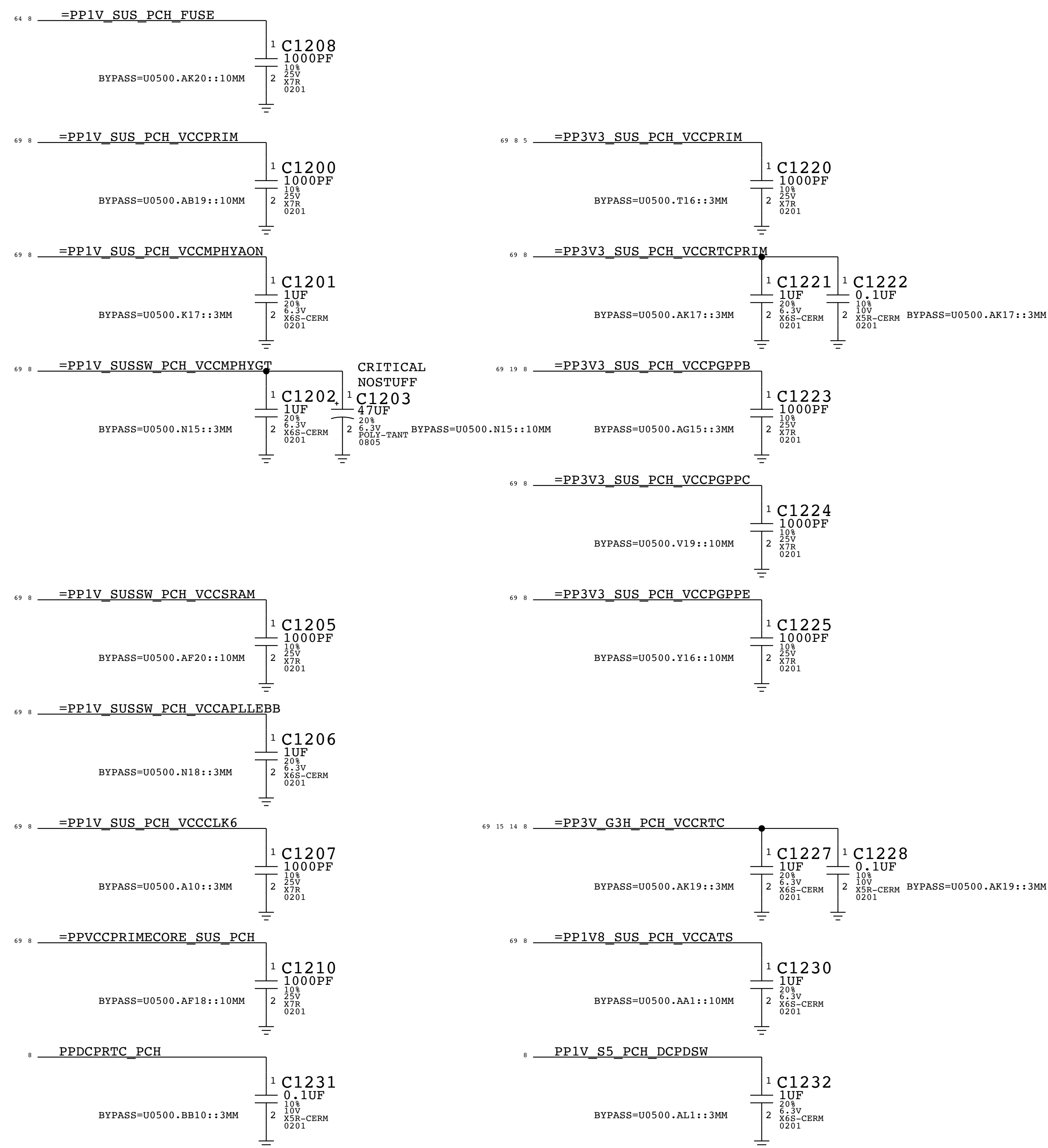
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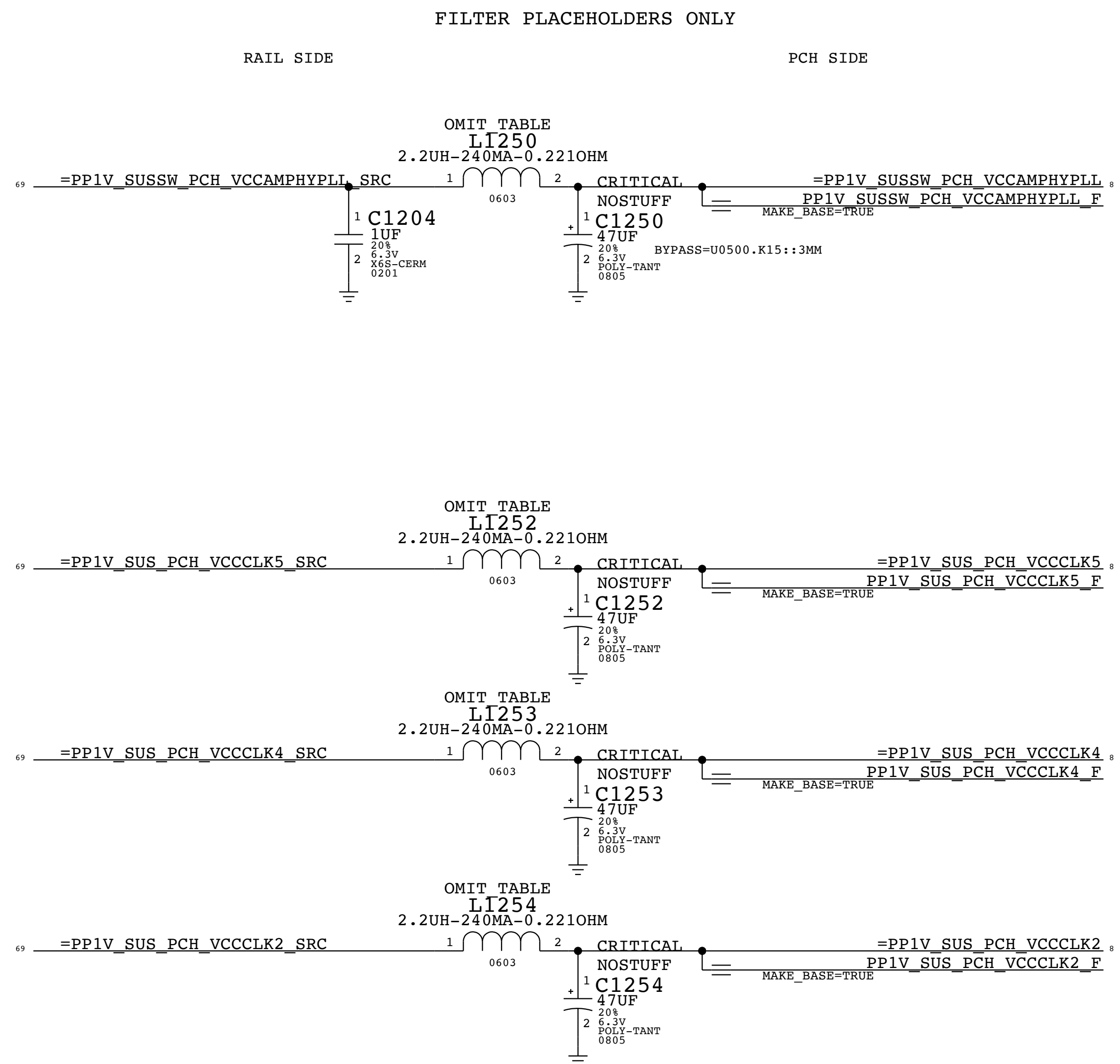
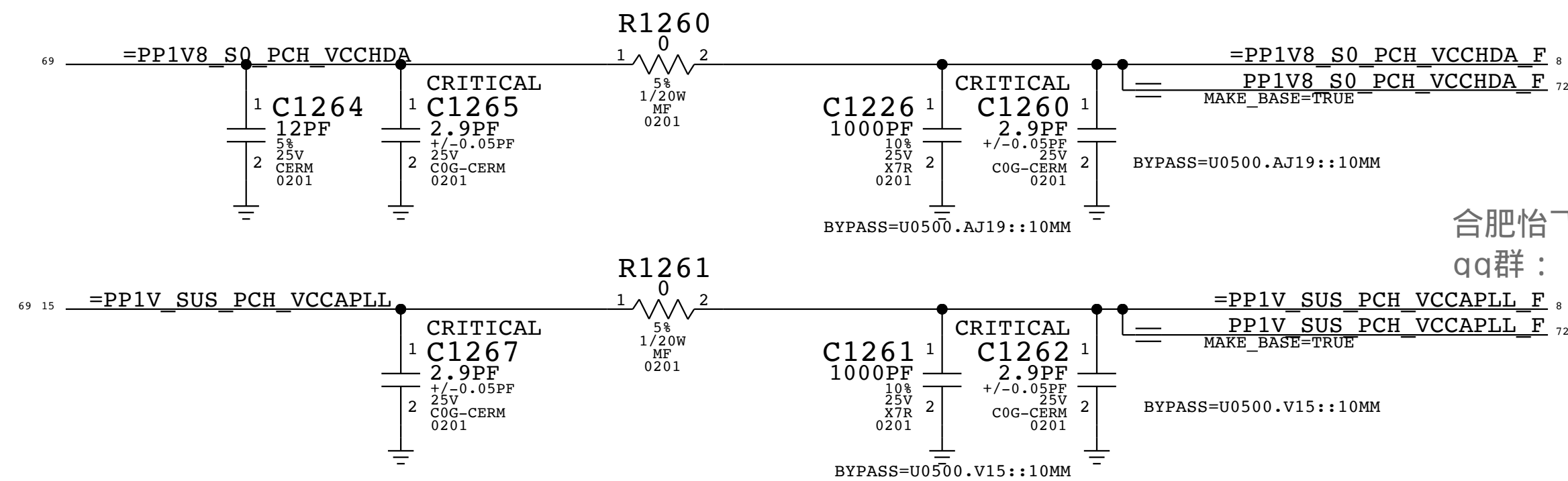
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PAGE TITLE		
CPU GT Decoupling		
 Apple Inc.	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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	PAGE	11 OF 500
	SHEET	11 OF 73

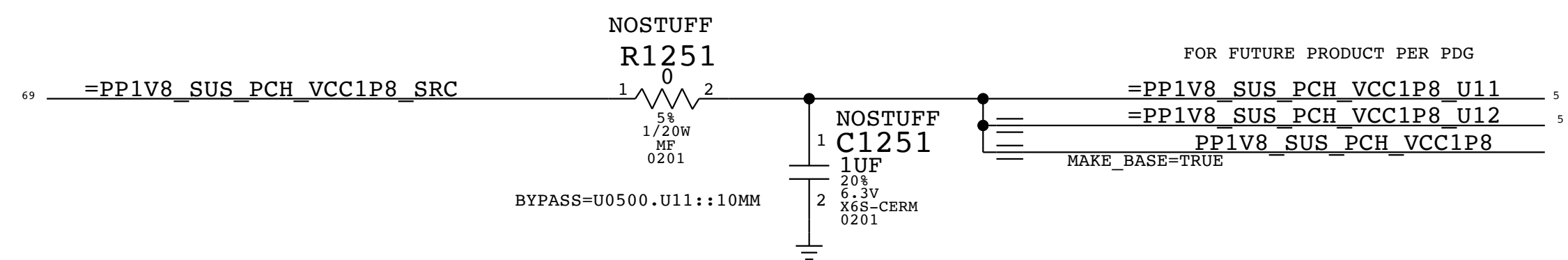
BOM\_COST\_GROUP=CPU & CHIPSET




CPU CIRCUITS GENERATE NOISE AT WIFI BAND FREQUENCIES.  
USE SPECIFIC 3PF CAPS FOR BEST FILTERING OF THOSE FREQUENCIES.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES,MF,1A MAX,00HM,5%,0603	L1250,L1252,L1253,L1254		



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PAGE TITLE		
PCH Decoupling		
 Apple Inc.	DRAWING NUMBER	SIZE
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	BRANCH	
	PAGE	
	12 OF 500	
	SHEET	
	12 OF 73	

BOM\_COST\_GROUP=CPU &amp; CHIPSET



D

C

B

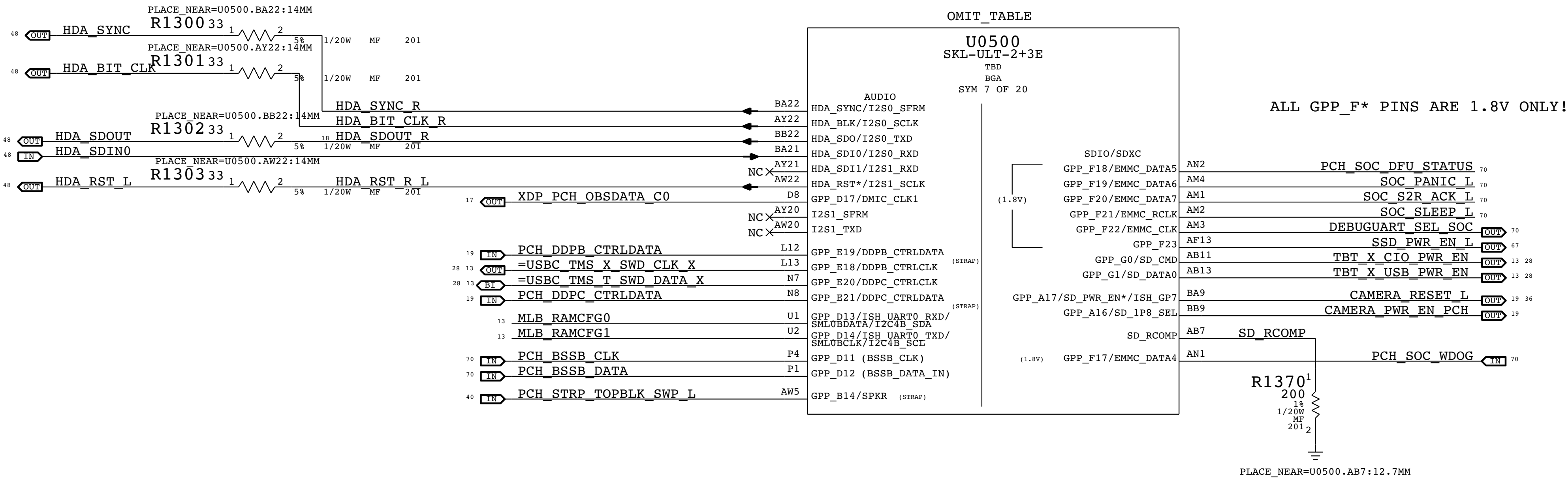
A

D

C

B

A



SOC\_ALS\_UART\_R2D

AD2

19

13

OUT

LCD\_PSR\_EN

AD3

19

13

OUT

PCH\_UART2\_CTS\_L

AD4

19

13

OUT

MLB\_RAMCFG2

U3

13

OUT

MLB\_RAMCFG3

U4

13

OUT

SOC\_ALS\_UART\_D2R

AD1

19

13

OUT

SPI\_CLK

AV2

47

OUT

SPI\_MISO

AW3

47

OUT

SPI\_MOSI

AW3

47

OUT

SPI\_IO&lt;2&gt;

AW2

47

OUT

SPI\_IO<3>

AW4

47

OUT

SPI\_CS0\*

AU3

47

OUT

SPI\_CS1\*

AU2

70

OUT

SPI\_CS2\*

AU1

70

OUT

OMIT\_TABLE

U0500

SKL-ULT-2+3E

TBD

BGA

SYM 5 OF 20

SPI\_FLASH

GPP\_C0/SMBCLK

R7

SMBUS\_PCH\_CLK

42

OUT

SMBUS\_SMLINK

GPP\_C1/SMBDATA

R8

SMBUS\_PCH\_DATA

42

OUT

GPP\_C2/SMBALERT\*

R10

TP\_PCH\_STRP\_TLSCONF

70

OUT

GPP\_C3/SML0CLK

R9

SML\_PCH\_0\_CLK

42

OUT

GPP\_C4/SML0DATA

W2

SML\_PCH\_0\_DATA

42

OUT

GPP\_C5/SML0ALERT\*

W1

TP\_PCH\_STRP\_ESPI

70

OUT

GPP\_C6/SML1CLK

W3

SML\_PCH\_1\_CLK

42

OUT

GPP\_C7/SML1DATA

V3

SML\_PCH\_1\_DATA

42

OUT

GPP\_B23/SML1ALERT\*/PCHHOT\*

AM7

PCH\_STRP\_BSSB\_SEL\_GPIO

19

OUT

LPC

GPP\_A1/LAD0/ESPI\_IO0

AY13

LPC\_AD\_R<0>

33

1

2

5%1/20W MF 201

LPC\_AD<0>

BT

39

GPP\_A2/LAD1/ESPI\_IO1

BA13

LPC\_AD\_R<1>

33

1

2

5%1/20W MF 201

LPC\_AD<1>

BT

39

GPP\_A3/LAD2/ESPI\_IO2

BB13

LPC\_AD\_R<2>

33

1

2

5%1/20W MF 201

LPC\_AD<2>

BT

39

GPP\_A4/LAD3/ESPI\_IO3

AY12

LPC\_AD\_R<3>

33

1

2

5%1/20W MF 201

LPC\_AD<3>

BT

39

GPP\_A5/LFRAME\*/ESPI\_CS\*

BA12

LPC\_FRAME\_R\_L

33

1

2

5%1/20W MF 201

LPC\_FRAME\_L

OUT

39

GPP\_A14/SUS\_STAT\*/ESPI\_RESET\*

BA11

LPC\_PWRDWN\_L

39

OUT

GPP\_A9/CLKOUT\_LPC0/ESPI\_CLK

AW9

LPC\_CLK24M\_SMC\_R

22

1

2

5%1/20W MF 201

LPC\_CLK24M\_SMC

OUT

39

GPP\_A10/CLKOUT\_LPC1

AY9

TP\_PCH\_CLKOUT\_LPC1

70

OUT

GPP\_A8/CLKRUN\*

AW11

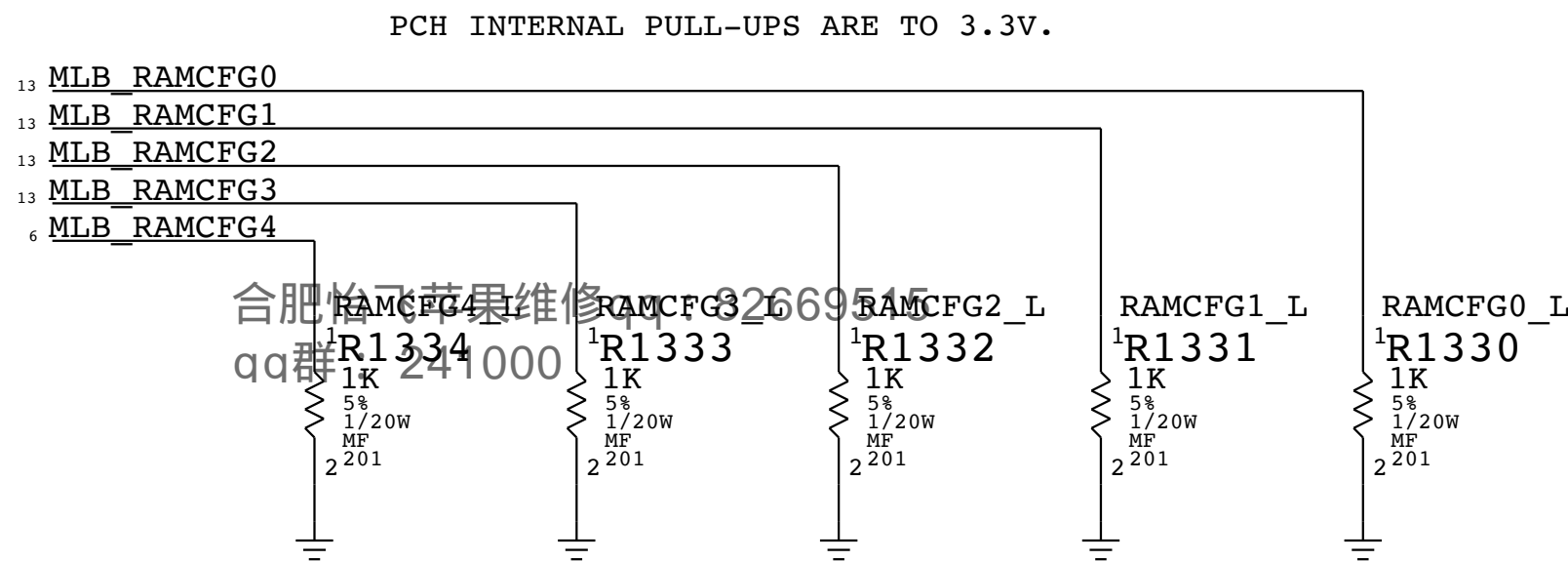
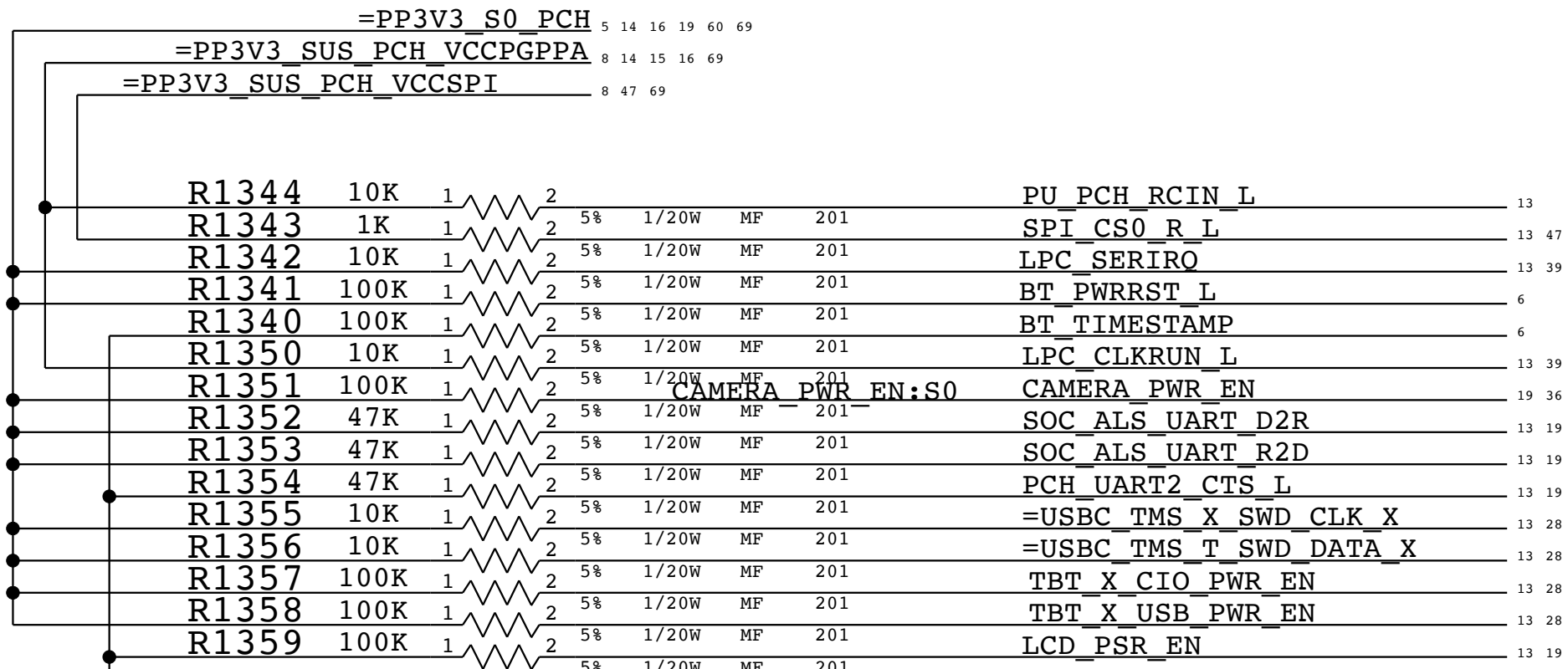
LPC\_CLKRUN\_L

13

39


OUT

### MEMORY CONFIGURATION STRAPS.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L, RAMCFG3_L, RAMCFG2_L, RAMCFG1_L, RAMCFG0_L

BOM\_COST\_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
PCH Audio/LPC/SPI/SMBus		
 Apple Inc.	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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	PAGE	13 OF 500
	SHEET	13 OF 73

D

C

B

A

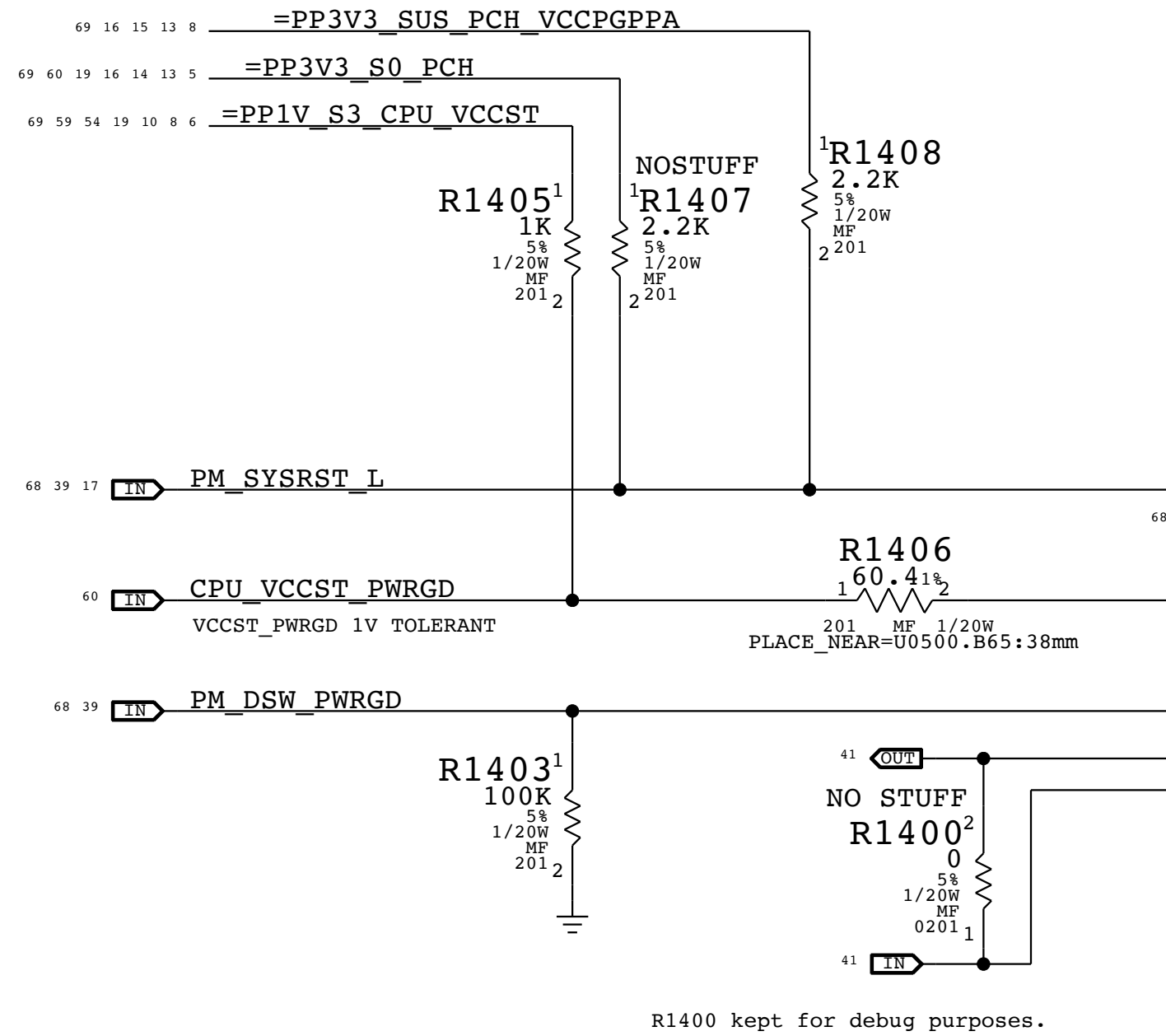
D

C

B

A

PCH Reset Button

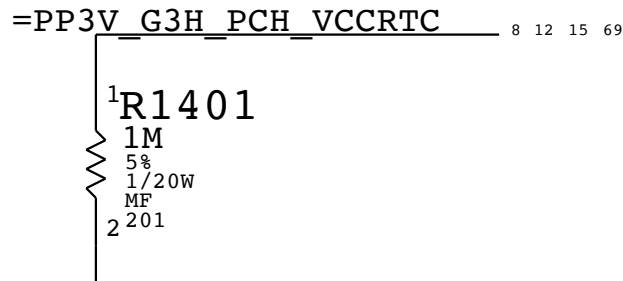


R1400 kept for debug purposes.

OMIT TABLE

U0500  
SKL-ULT-2+3E  
TBD  
BGA  
SYM 11 OF 20  
SYSTEM POWER MANAGEMENT

GPP_B12/SLP_S0*	AT11	PM_SLP_S0_L	14 39 60 72
GPD4/SLP_S3*	AP15	PM_SLP_S3_L	14 26 39 59 60 66 72
GPD5/SLP_S4*	BA16	PM_SLP_S4_L	14 39 60 68 72
GPD10/SLP_S5*	AY16	PM_SLP_S5_L	14 39 60 72
SLP_SUS*	AN15	PM_SLP_SUS_L	14 60 72
SLP_LAN*	AW15		
GPD9/SLP_WLAN*	BB17	TP_PCH_SLP_WLAN_L	70
GPD6/SLP_A*	AN16	TP_PCH_SLP_A_L	72
GPD3/PWRBTN*	BA15	PCH_PWRBTN_L	14 41
GPD1/ACPRESENT*	AY15	SSD_SR_EN_L	14 67
GPD0/BATLOW*	AU13	PM_BATLOW_L	14 28 39
GPP_A11/PME*	AU11	TP_PCH_PME_L	70
INTRUDER*	AP16	PCH_INTRUDER_L	
GPP_B11/EXT_PWR_GATE*	AM10	PCH_HSIO_PWR_EN	60
GPP_B2/VRALER*	AM11	BT_LOW_PWR_L	14 34 35



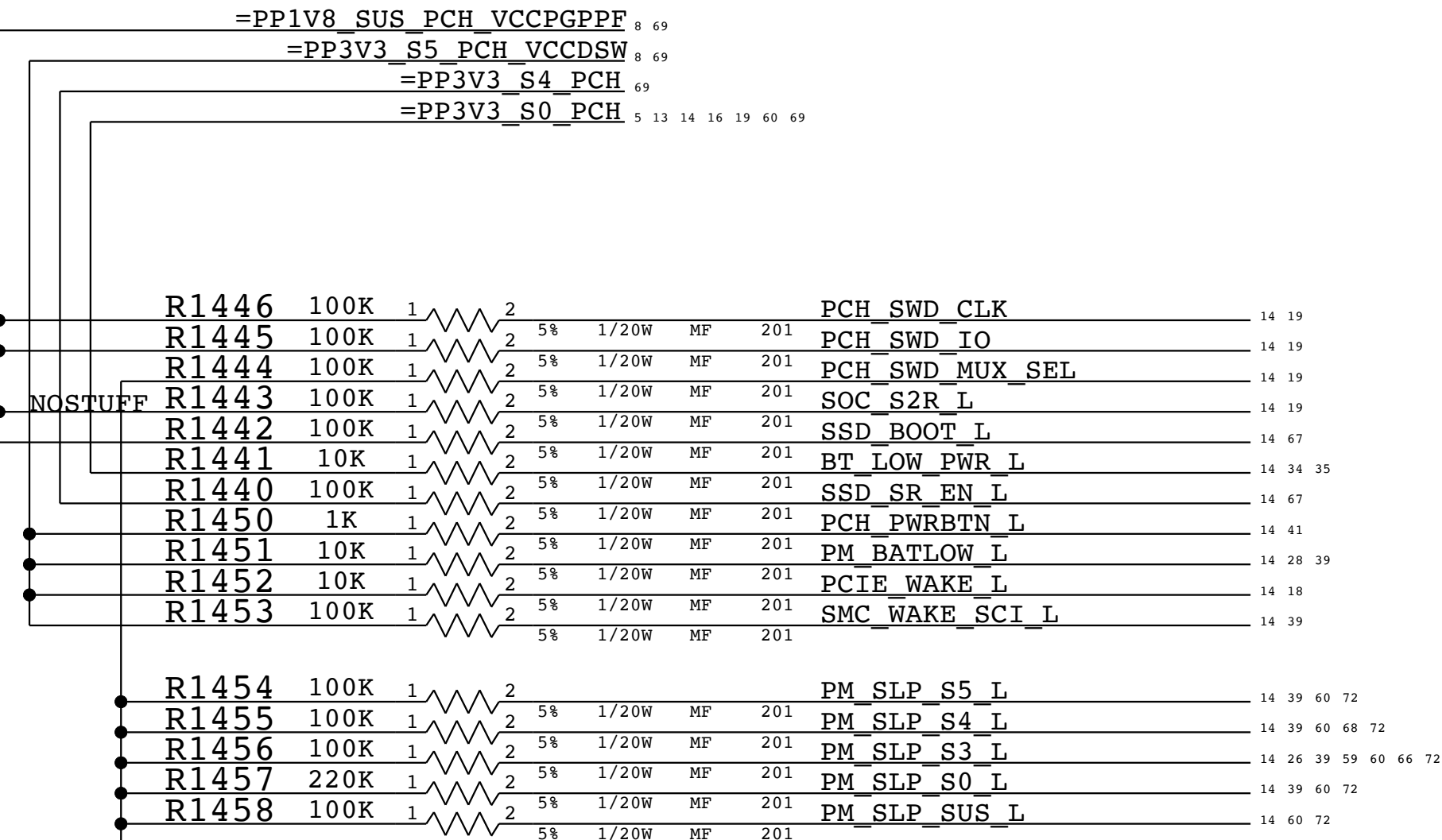
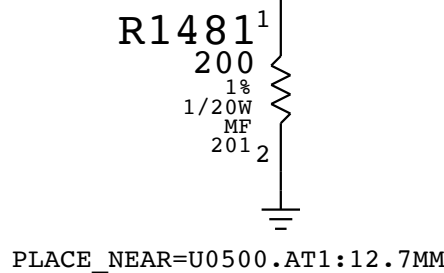
OMIT TABLE  
U0500  
SKL-ULT-2+3E  
TBD  
BGA  
SYM 9 OF 20

CSI2_DN0	C37	CSI2_CLKN0	XNC
CSI2_DP0	D37	CSI2_CLKP0	XNC
CSI2_DN1	C32	CSI2_CLKN1	XNC
CSI2_DP1	D32	CSI2_CLKP1	XNC
CSI2_DN2	C29	CSI2_CLKN2	XNC
CSI2_DP2	D29	CSI2_CLKP2	XNC
CSI2_DN3	B26	CSI2_CLKN3	XNC
CSI2_DP3	A26	CSI2_CLKP3	XNC
CSI2_DN4	E13	CSI2_COMP	
CSI2_DP4	M1	TP_PCH_GPP_D0	70
CSI2_DN5			
CSI2_DP5			
CSI2_DN6			
CSI2_DP6			
CSI2_DN7			
CSI2_DP7			
CSI2_DN8			
CSI2_DP8			
CSI2_DN9			
CSI2_DP9			
CSI2_DN10			
CSI2_DP10			
CSI2_DN11			
CSI2_DP11			

ALL GPP F\* PINS ARE 1.8V ONLY!

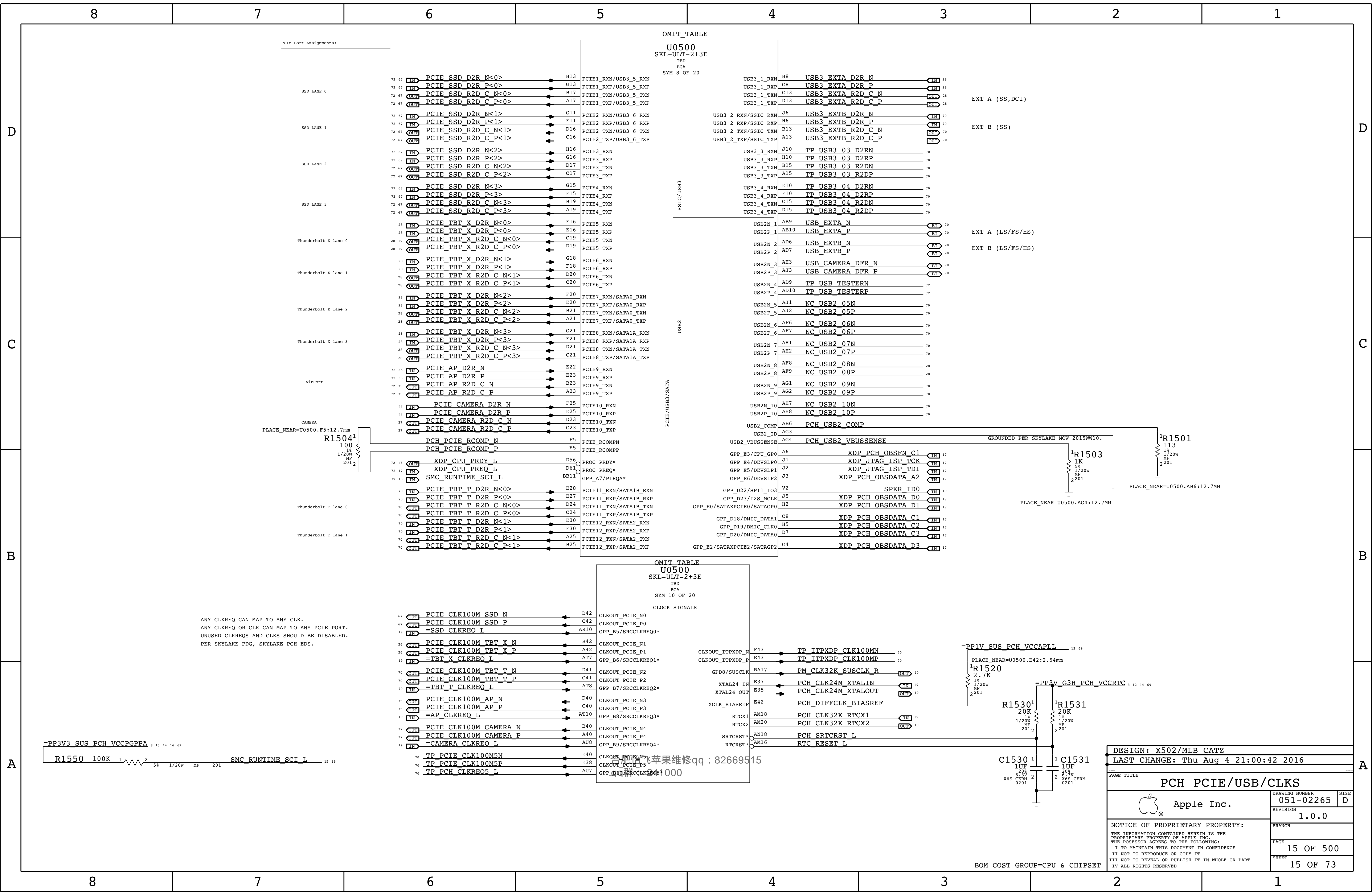
GPP_F7/I2C3_SCL	AH12	SSD_BOOT_L	14 67
GPP_F8/I2C4_SDA	AF11	TP_PCH_GPP_F8	70
GPP_F9/I2C4_SCL	AF12	TP_PCH_GPP_F9	70
GPP_F10/I2C5_SDA/ISH_I2C2_SDA	AD11	TP_PCH_GPP_F10	70
GPP_F11/I2C5_SCL/ISH_I2C2_SCL	AD12	PCH_BT_ROM_BOOT	70
GPP_F12/EMMC_CMD	AP4	PCH_SWD_CLK	14 19
GPP_F13/EMMC_DATA0	AP2	PCH_SWD_IO	14 19
GPP_F14/EMMC_DATA1	AP1	PCH_SWD_MUX_SEL	14 19
GPP_F15/EMMC_DATA2	AP3	SOC_S2R_L	14 19
GPP_F16/EMMC_DATA3	AN3	PCH_SOC_FORCE_DFU	70
GPP_F6/I2C3_SDA	AH11	UPC_I2C_INT_L	70

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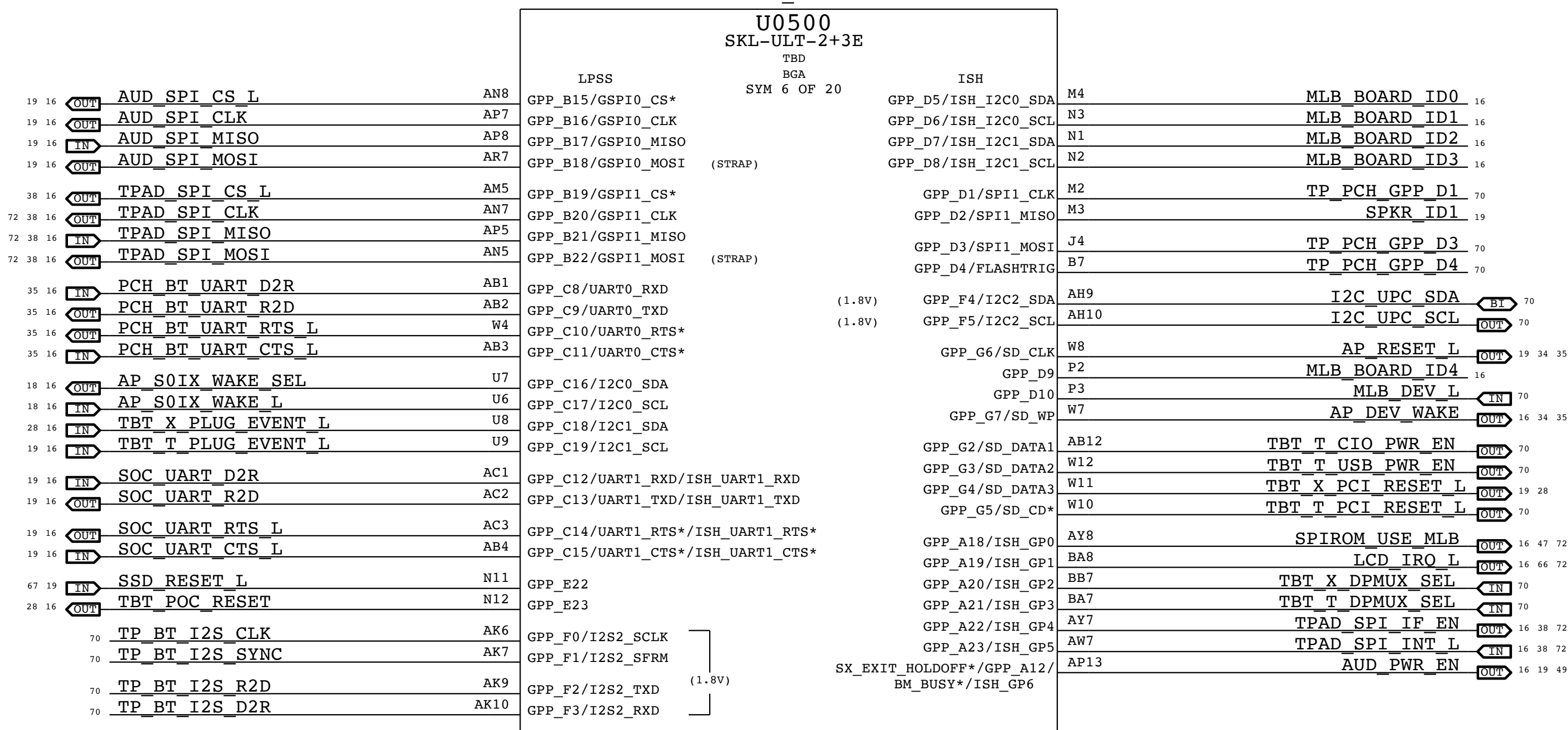


NOTE: PM\_SLP\_S0\_L HAS INTERNAL PULL-UP BEFORE RSMRST\_L IS RELEASED.  
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.  
THE SIGNAL IS DRIVEN HI AFTER RSMRST\_L IS RELEASED.

BOM\_COST\_GROUP=CPU & CHIPSET

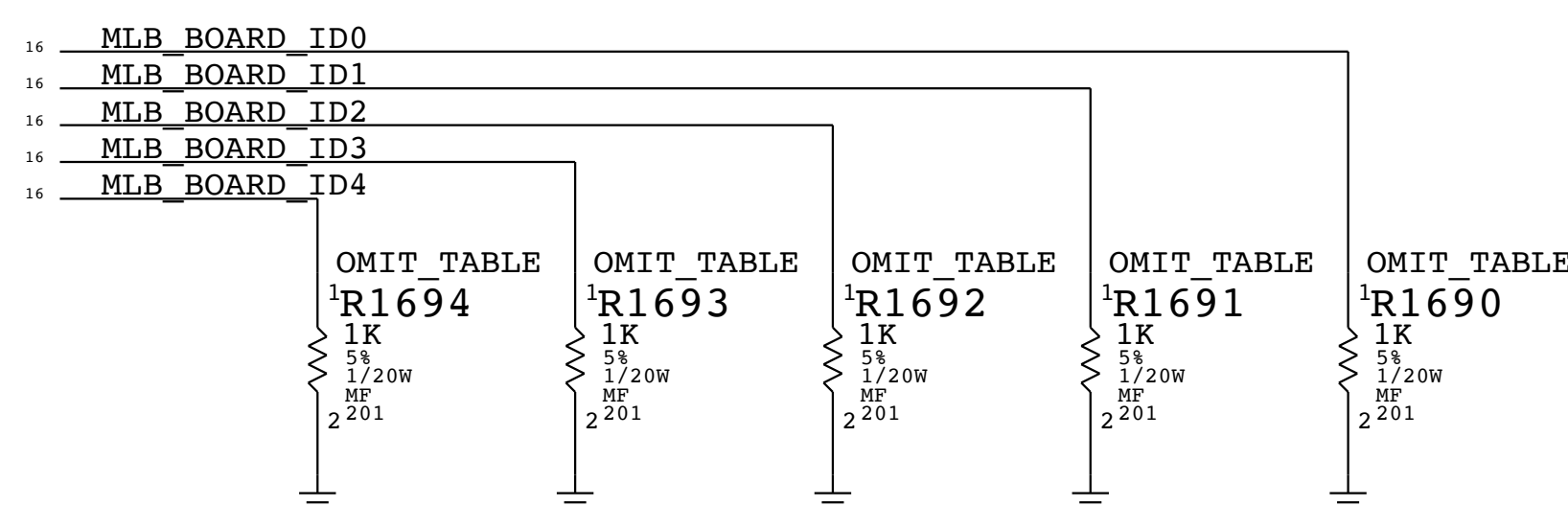


ALL GPP\_F\* PINS ARE 1.8V ONLY!  
OMIT TABLE




MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

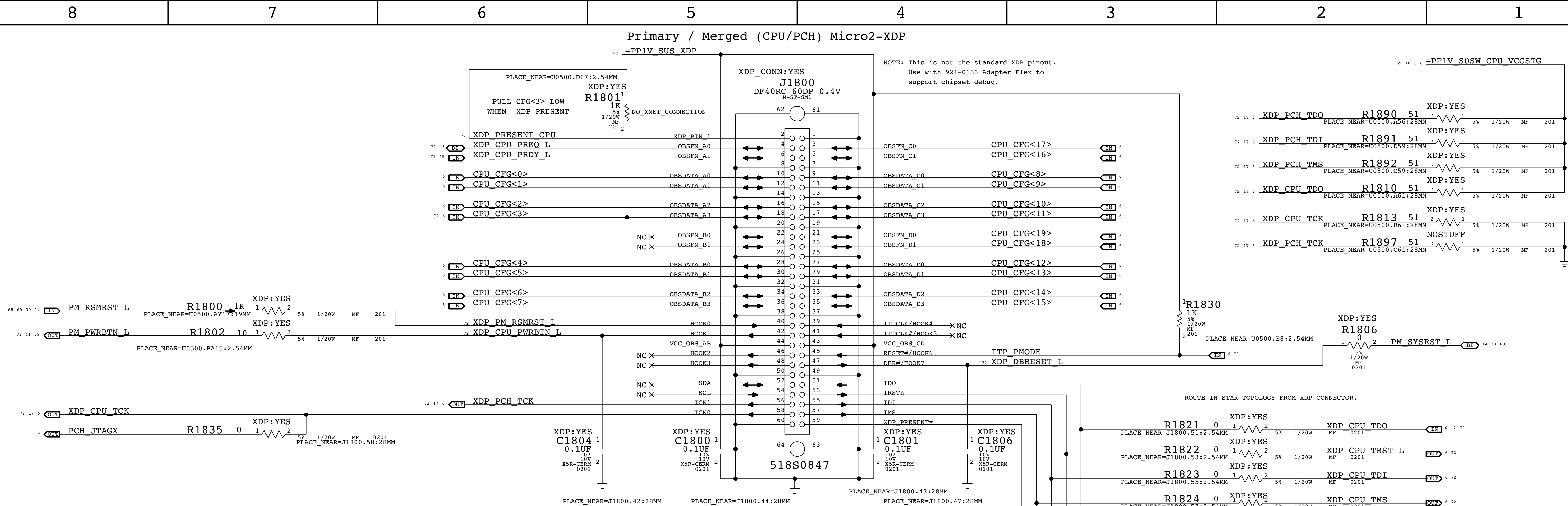


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>

DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
PCH SPI/UART/GPIO		
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BOM\_COST\_GROUP=CPU &amp; CHIPSET





## PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture. The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation. They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

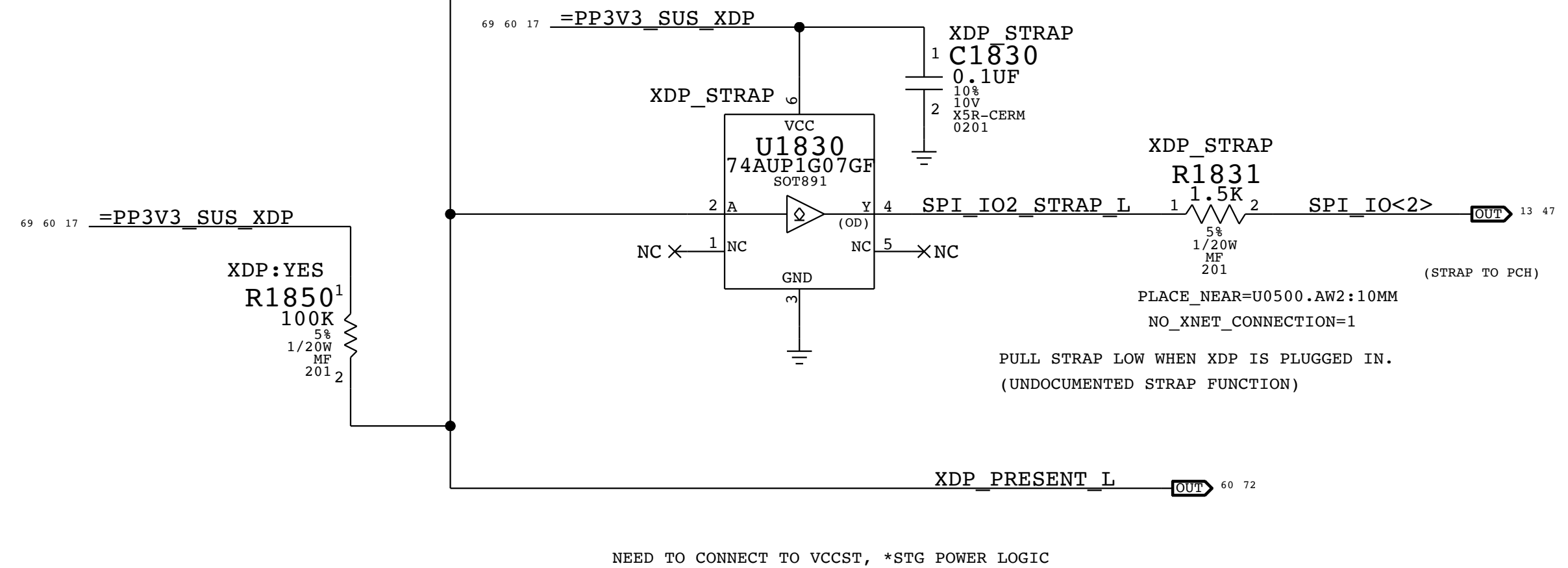
PCH/XDP Signals				Non-XDP Signals			
15	TP	XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE	==	JTAG_ISP_TCK	OUTP	28
15	TP	XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE	==	JTAG_ISP_TDI	OUTP	28
15	B1	XDP_PCH_OBSDATA_A2			TP	TP1870	
	B1	XDP_PCH_OBSDATA_A3			TP	TP1871	
5	B1	XDP_PCH_OBSDATA_B0			TP	TP1872	
13	B1	XDP_PCH_OBSDATA_C0			TP	TP1873	
15	B1	XDP_PCH_OBSDATA_C1			TP	TP1874	
15	B1	XDP_PCH_OBSDATA_C2			TP	TP1875	
15	B1	XDP_PCH_OBSDATA_C3			TP	TP1876	
	B1	XDP_PCH_OBSDATA_D0			TP	TP1877	
15	B1	XDP_PCH_OBSDATA_D1			TP	TP1878	
6	B1	XDP_PCH_OBSDATA_D2			TP	TP1879	
15	B1	XDP_PCH_OBSDATA_D3			TP	TP1880	
15	B1	XDP_PCH_OBSFN_C1			TP	TP1881	
5	OUTP	XDP_USB_EXT_A_OC_L	MAKE_BASE=TRUE	==	USB_EXT_A_OC_L	IN	28
5	OUTP	XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	==	USB_EXTB_OC_L	IN	28
5	OUTP	XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE	==	USB_EXTC_OC_L	IN	28
5	OUTP	XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE	==	USB_EXTD_OC_L	IN	28

Unused GPIOs have TPs.


USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG\_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

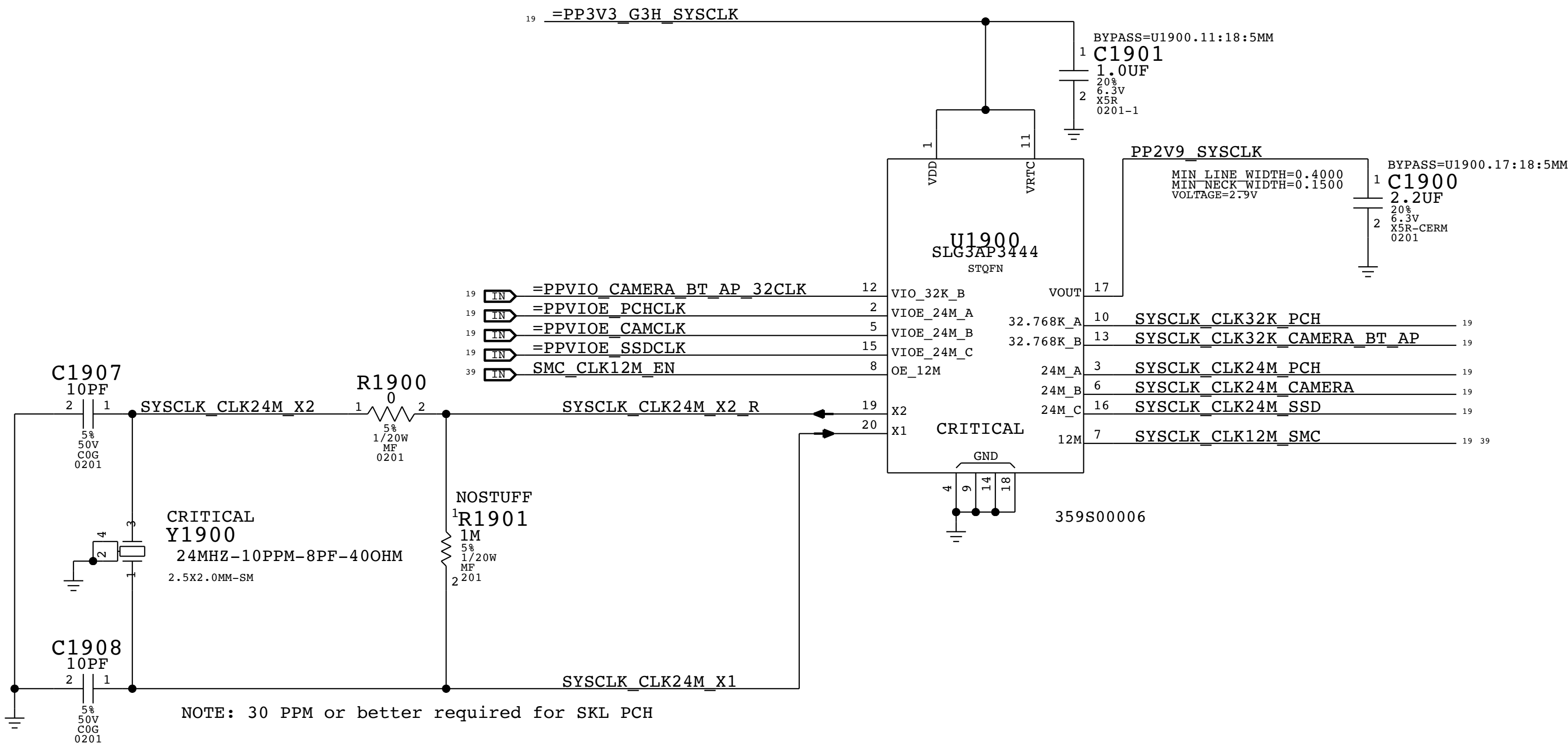
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qq群 : 241000



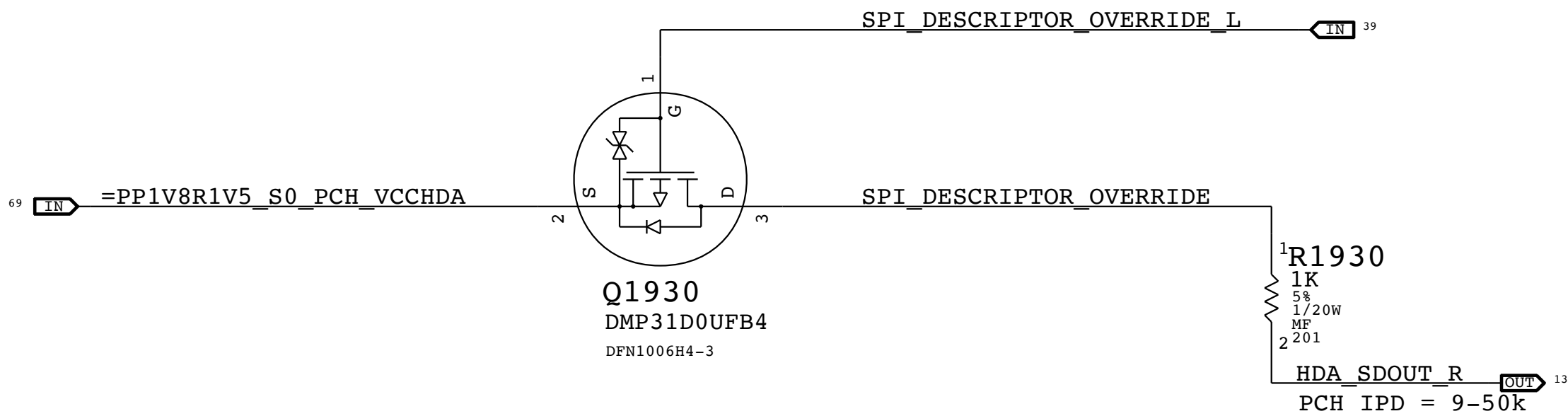
NEED TO CONNECT TO VCCST, \*STG POWER LOGIC

DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
CPU/PCH Merged XDP		
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	PAGE	18 OF 500
	SHEET	17 OF 73

System 32kHz / 12MHz / 24MHz Clock Generator

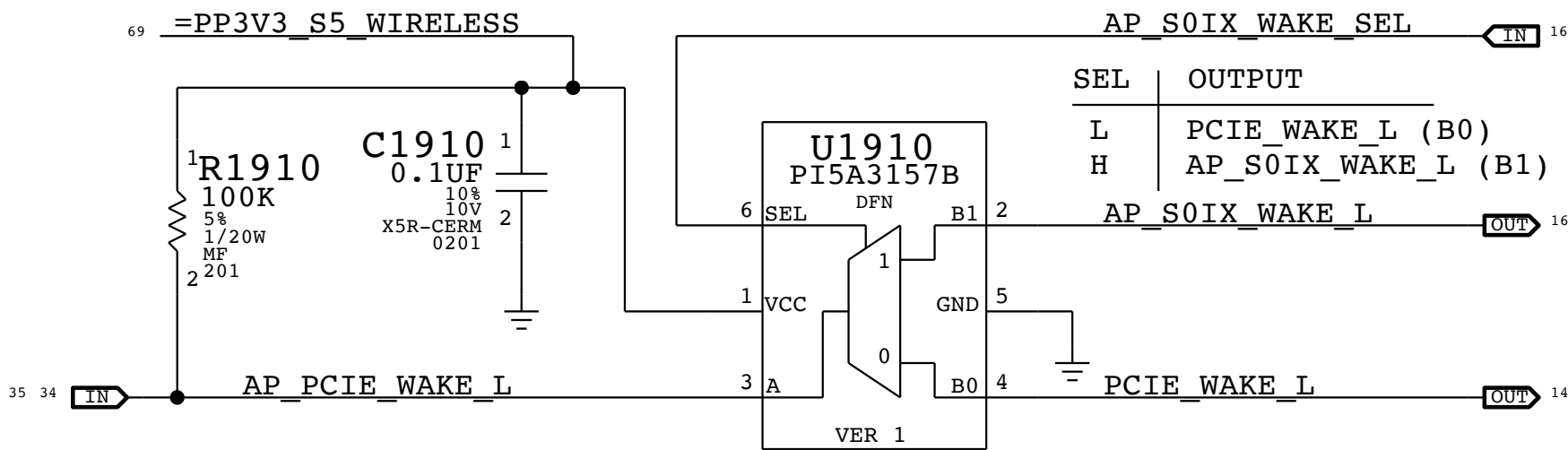


PCH ME Disable Strap



PCH uses HDA\_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. \*\*\*\*\* Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



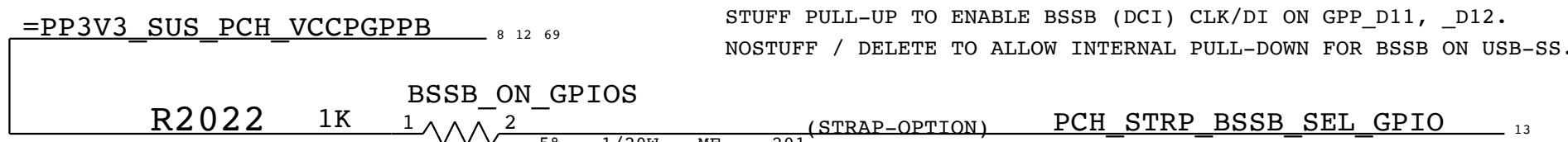
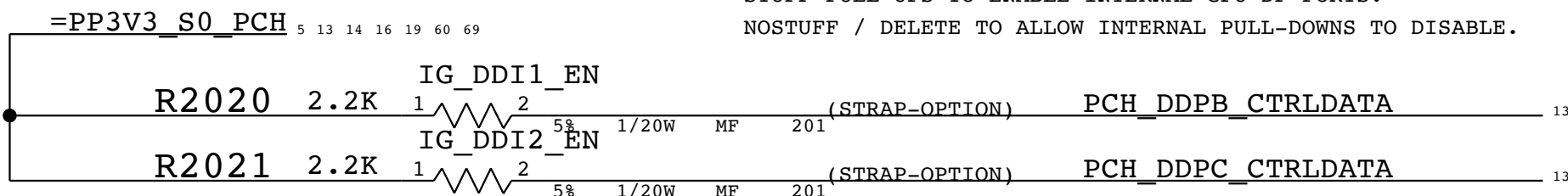
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PAGE TITLE			Chipset Support 1		
		DRAWING NUMBER		SIZE	
		051-02265		D	
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		BRANCH			
		PAGE		19 OF 500	
		SHEET		18 OF 73	

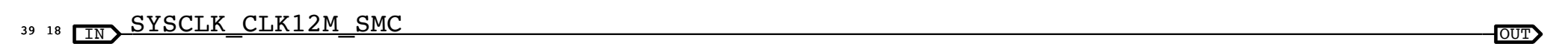
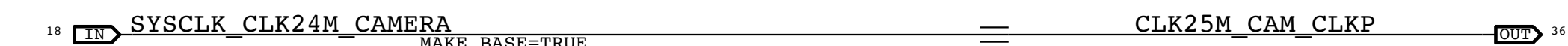
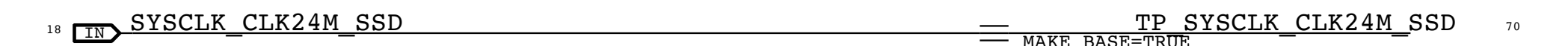
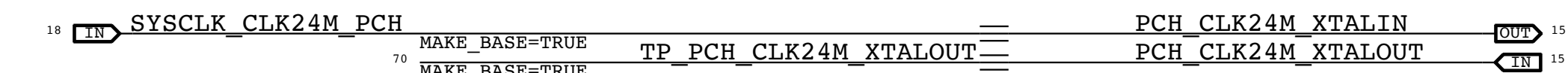
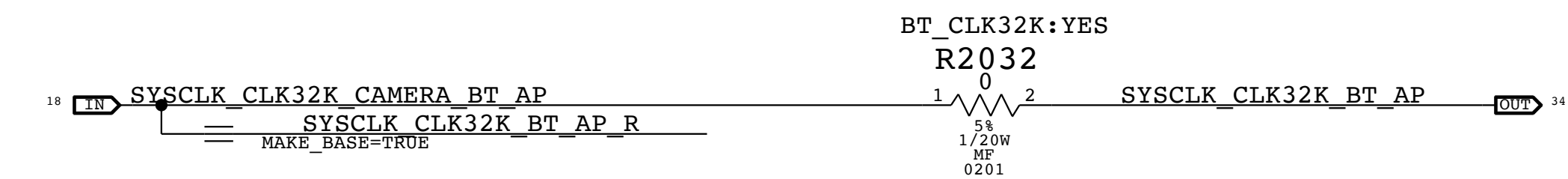
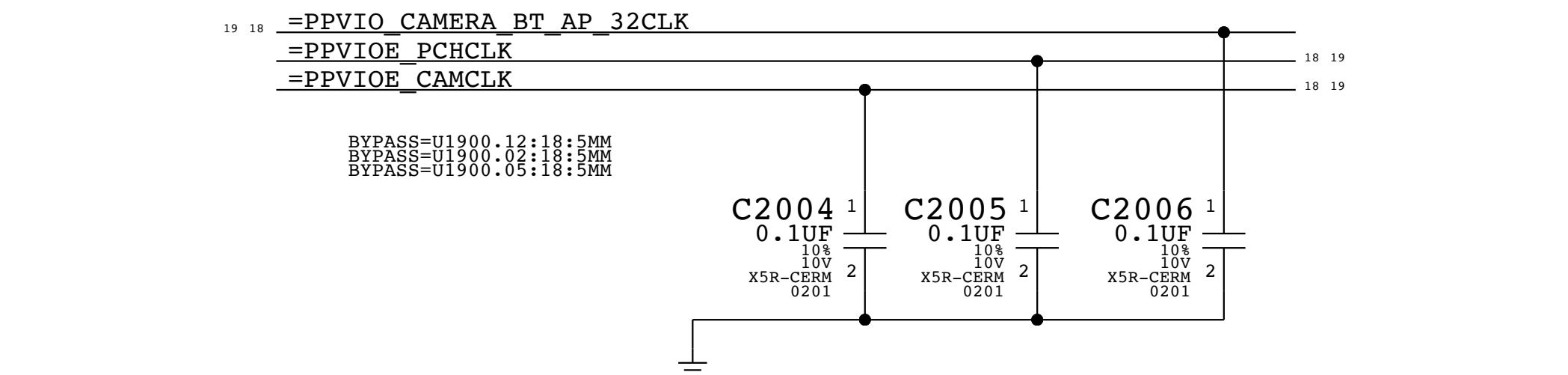
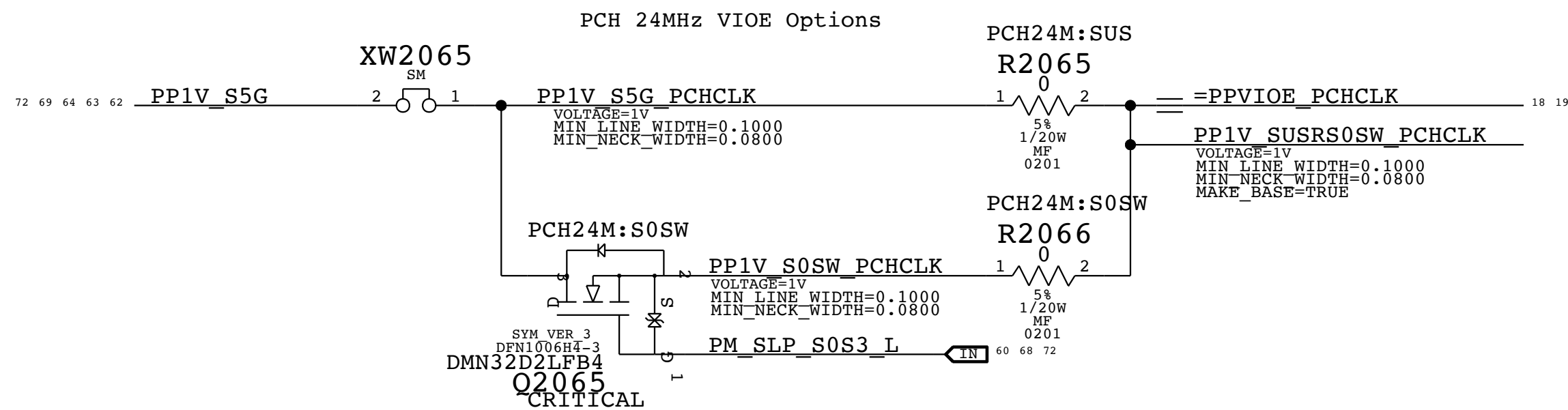
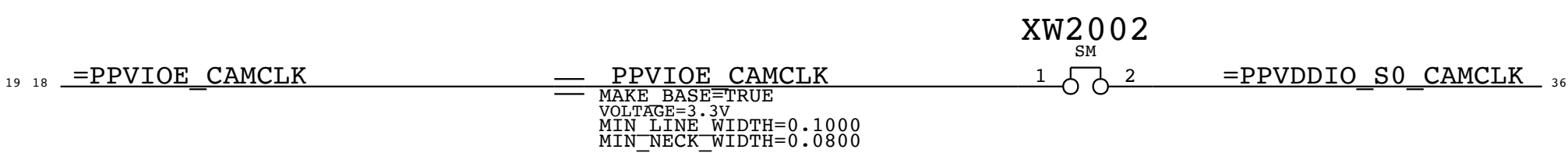
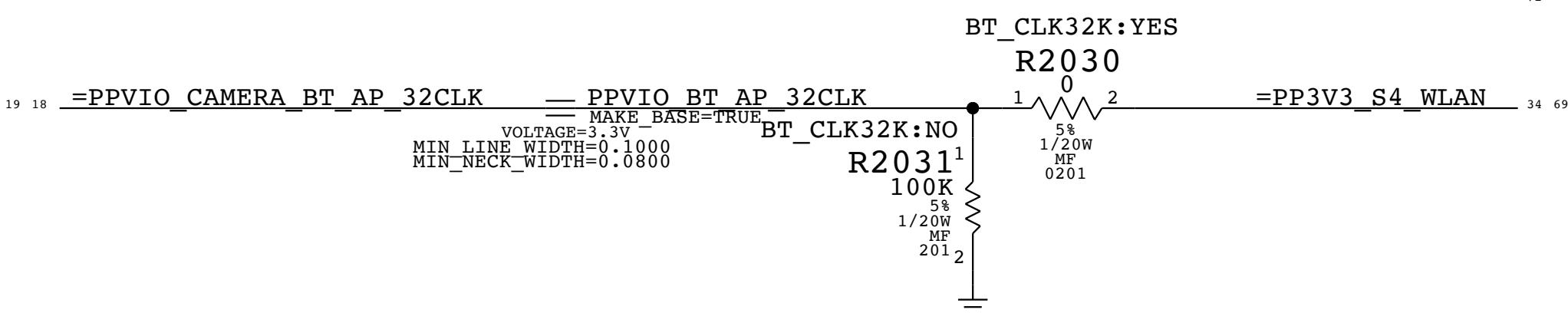
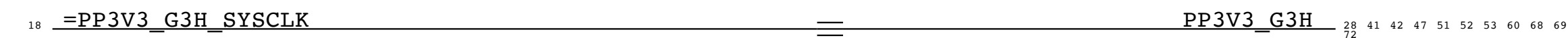
## OPTION STRAPS

PROJECT DEPENDANT

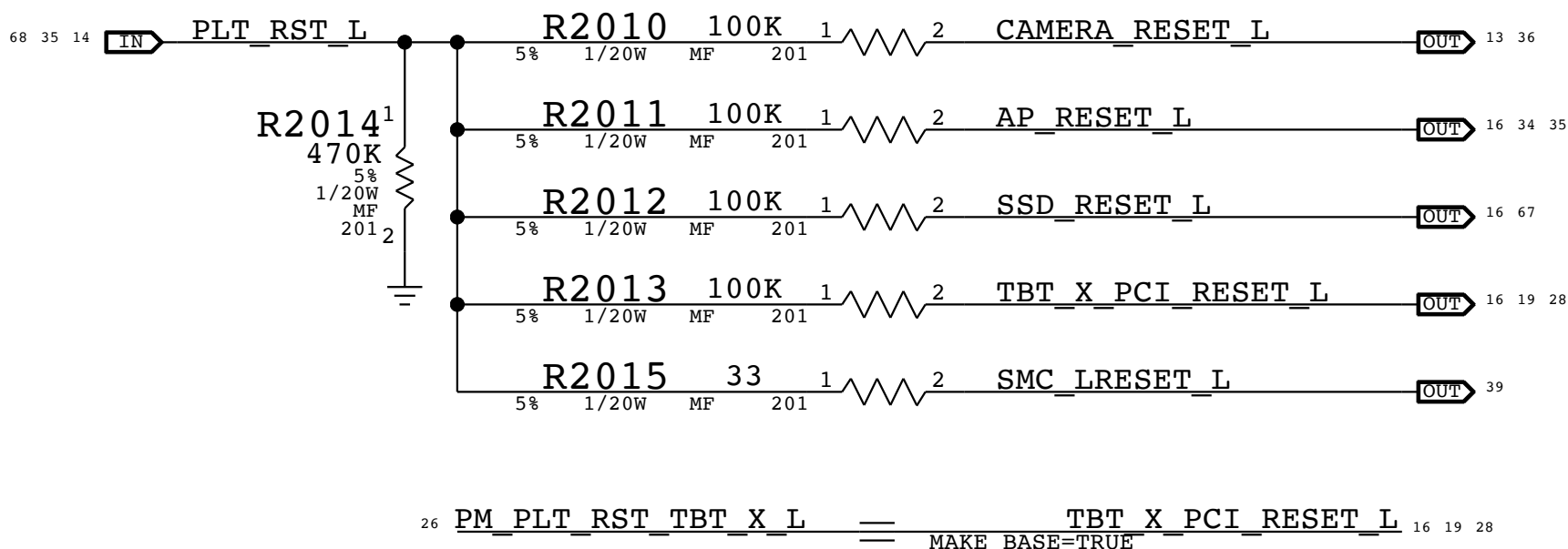
STUFF PULL-UPS TO ENABLE INTERNAL GPU DP PORTS.  
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWNS TO DISABLE.



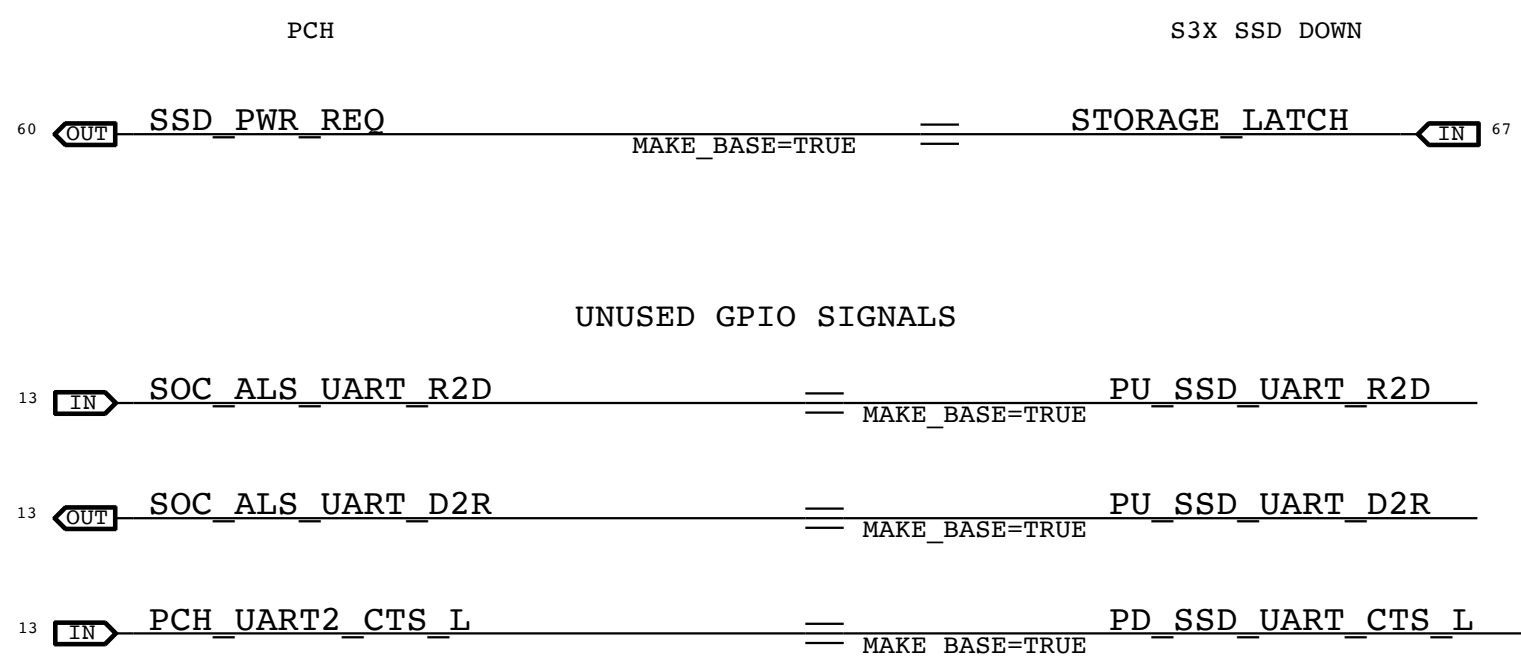
## GREENCLK CLOCK CONNECTIONS.



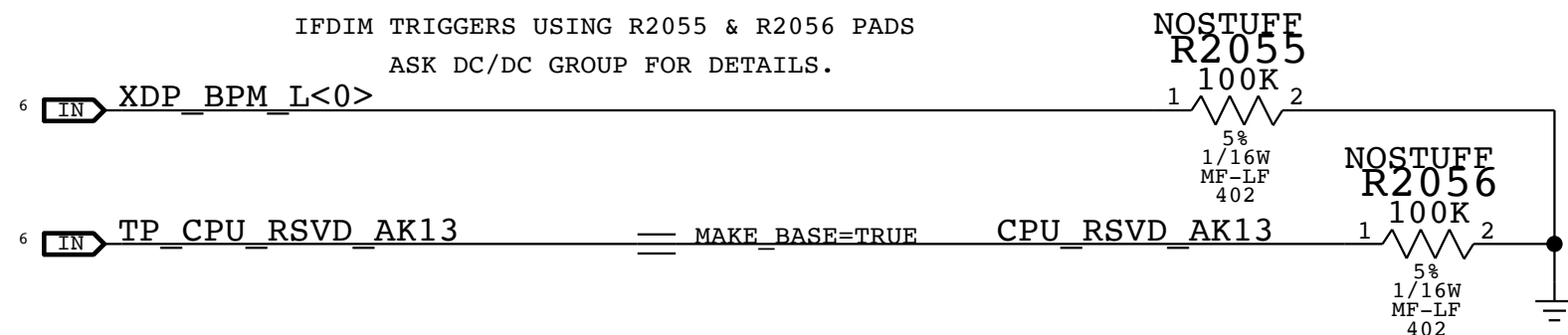
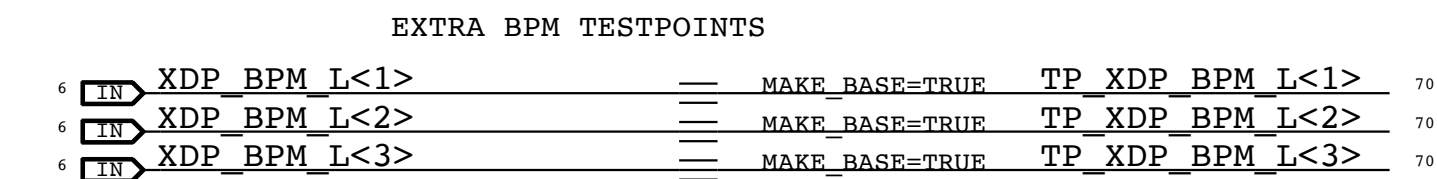
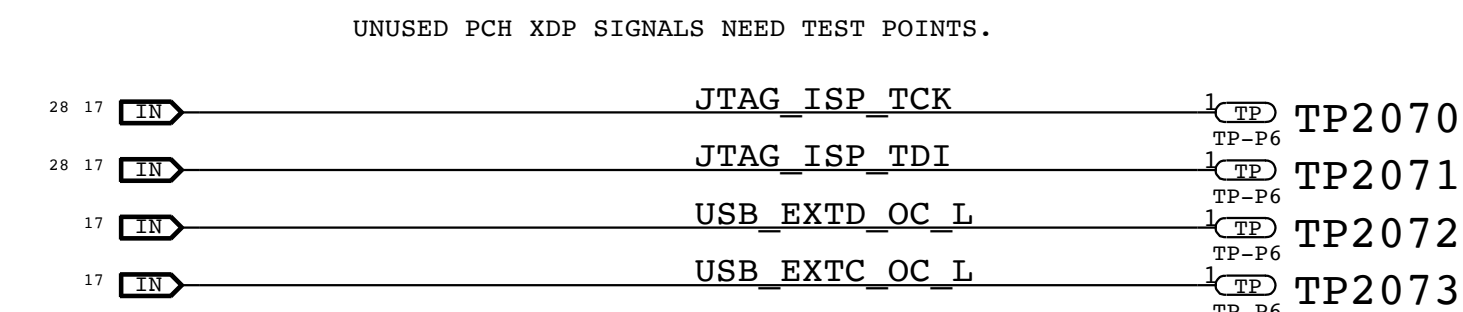
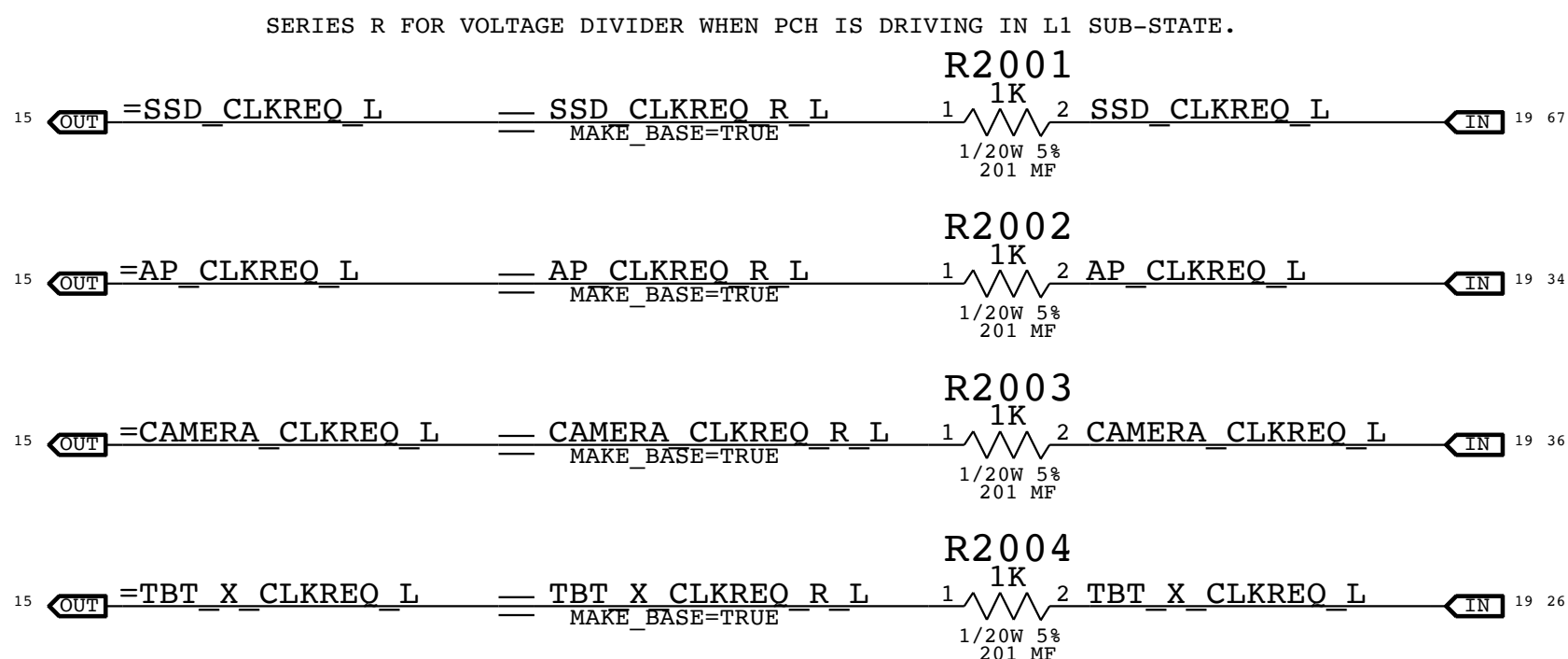
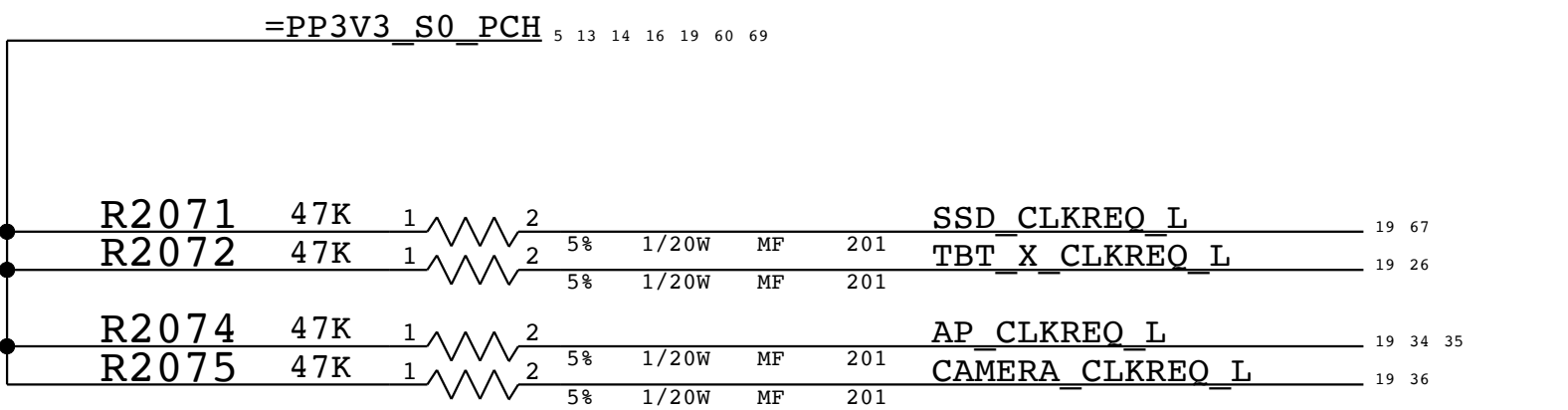
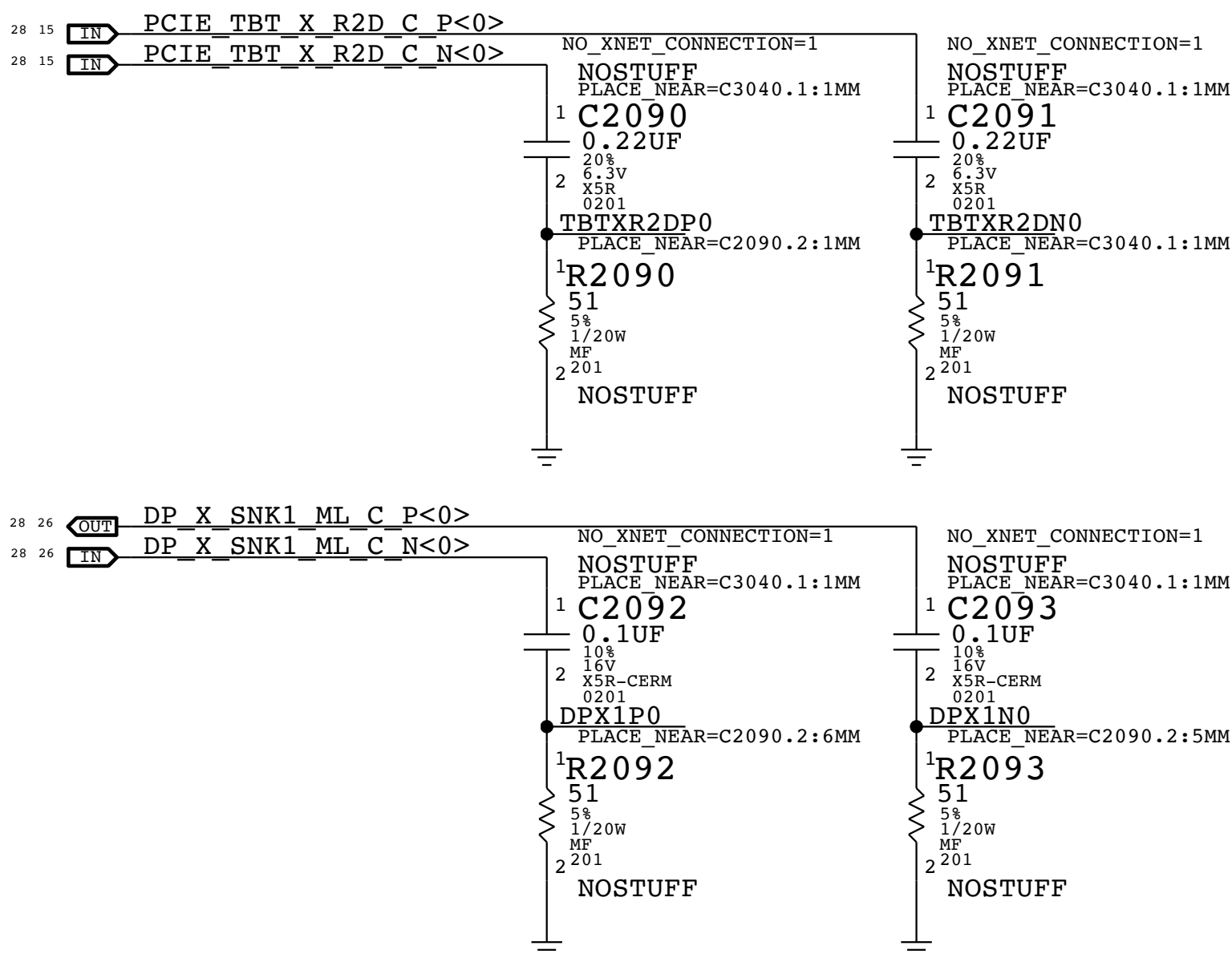
## RESETS



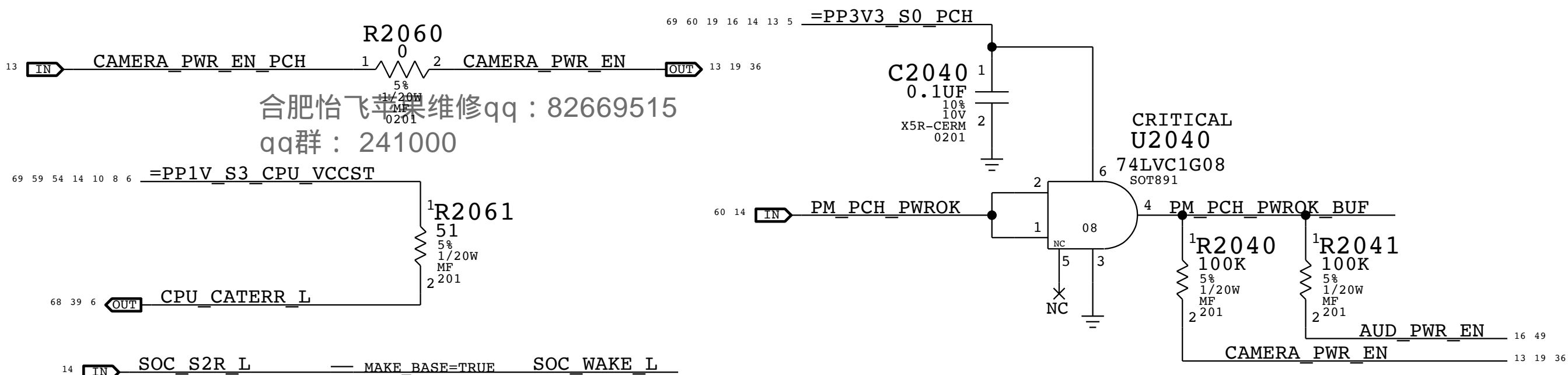
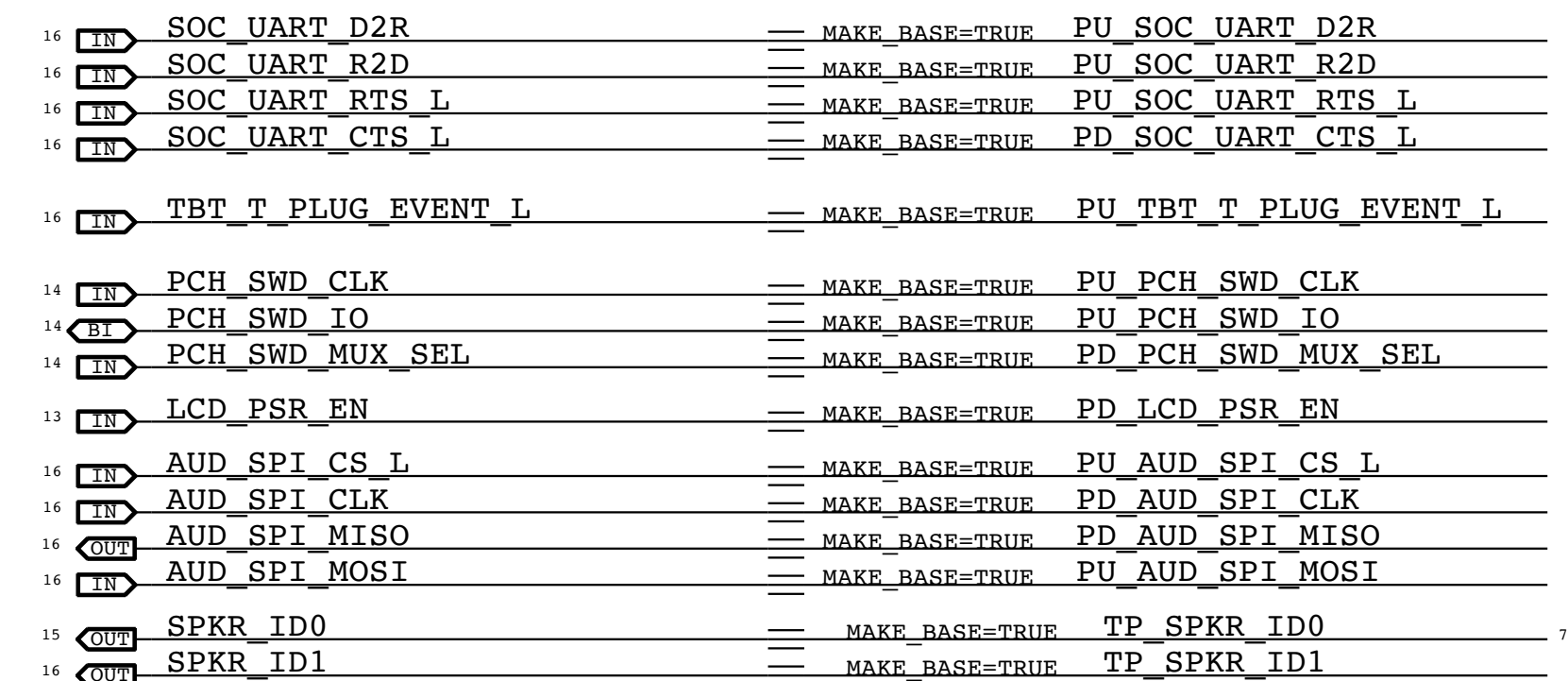
## S3X SSD CONTROL




## PROBE POINTS



## UNUSED GPIO SIGNALS

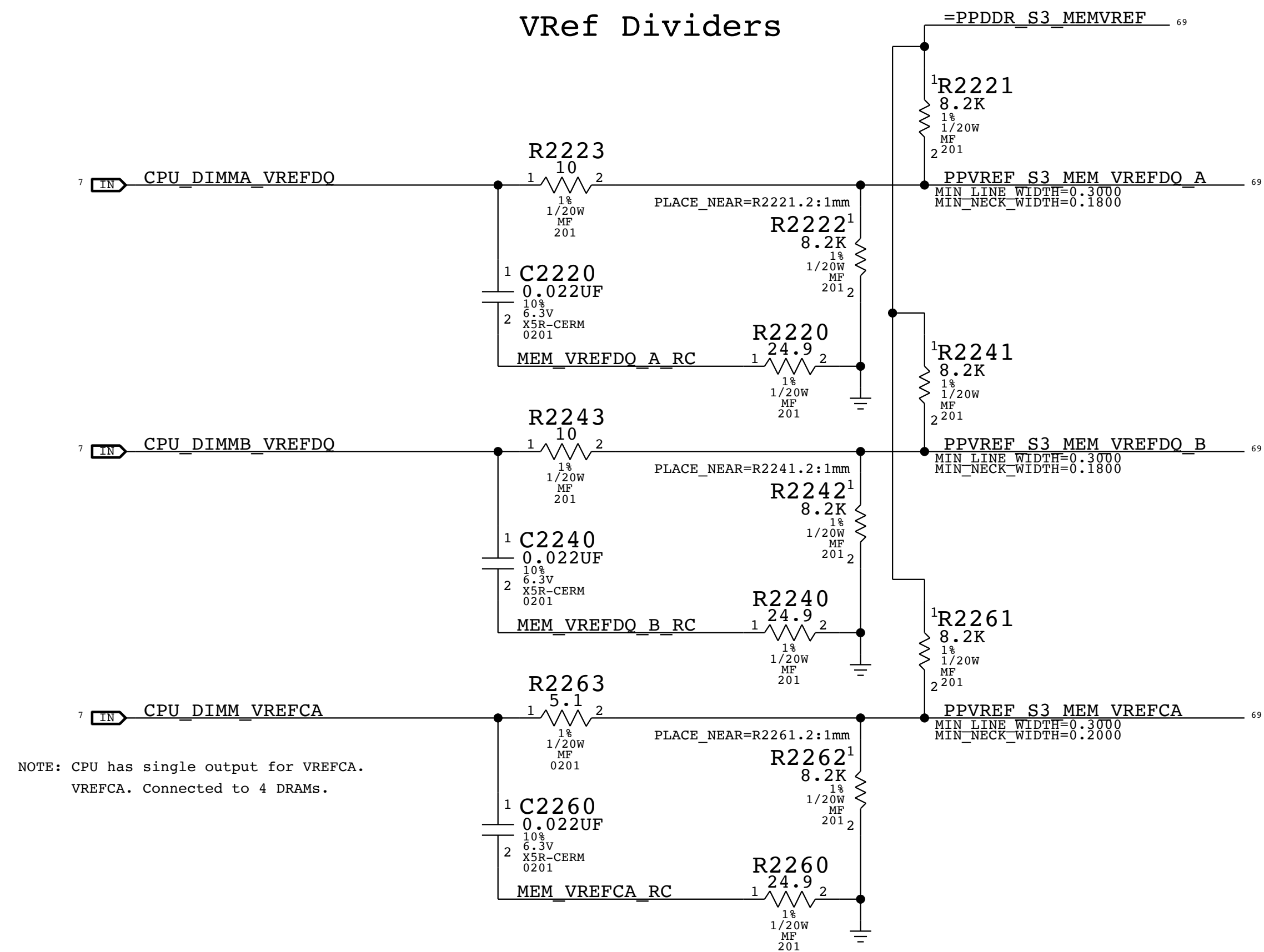


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qq群 : 241000


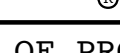
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LAST CHANGE: Thu Aug 4 21:00:42 2016		
PAGE TITLE		
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 Apple Inc.	DRAWING NUMBER	051-02265
	REVISION	1.0.0
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	PAGE	20 OF 500
	SHEET	19 OF 73

BOM\_COST\_GROUP=CPU & CHIPSET

## CPU-Based Margining

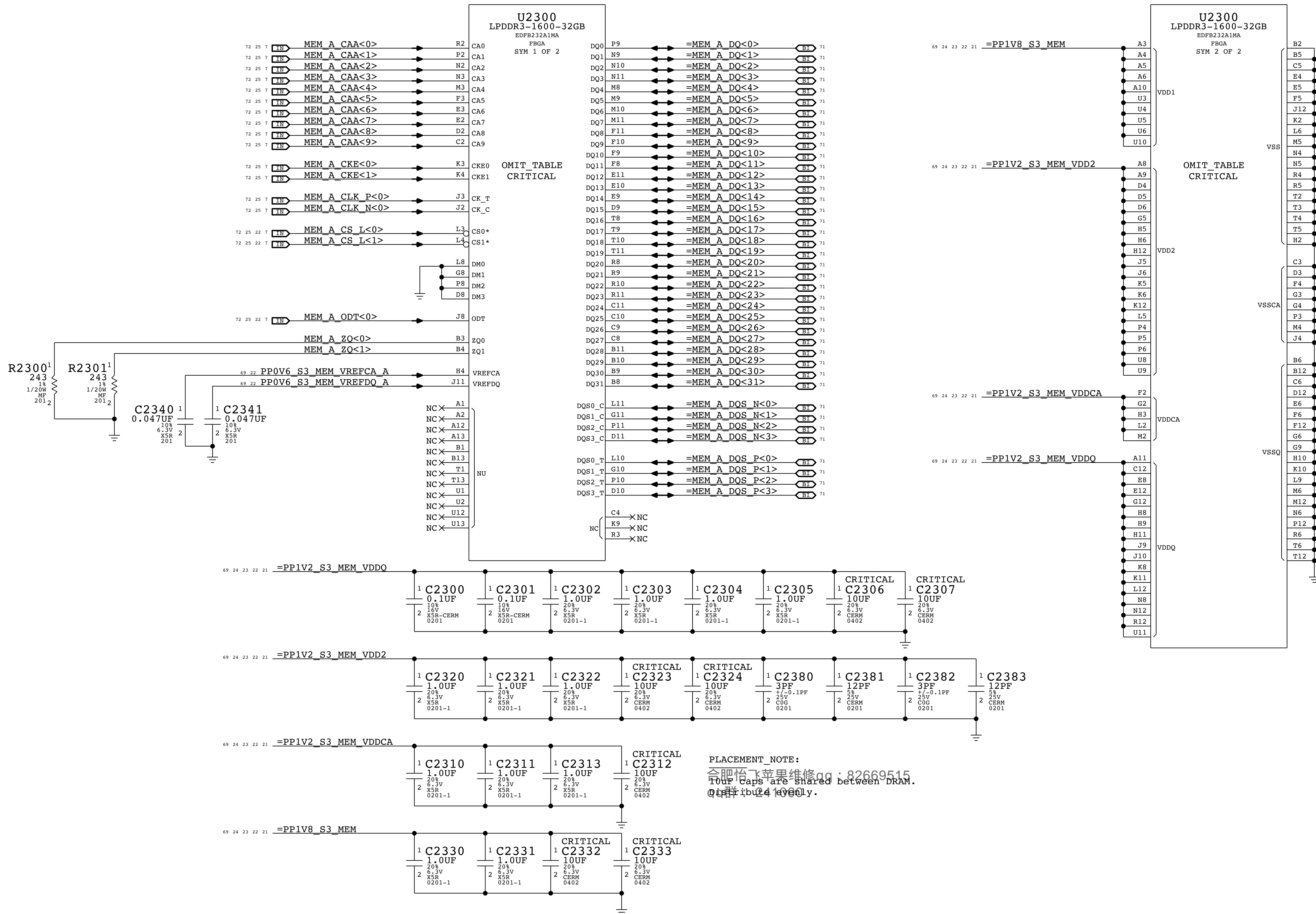


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qq群：241000

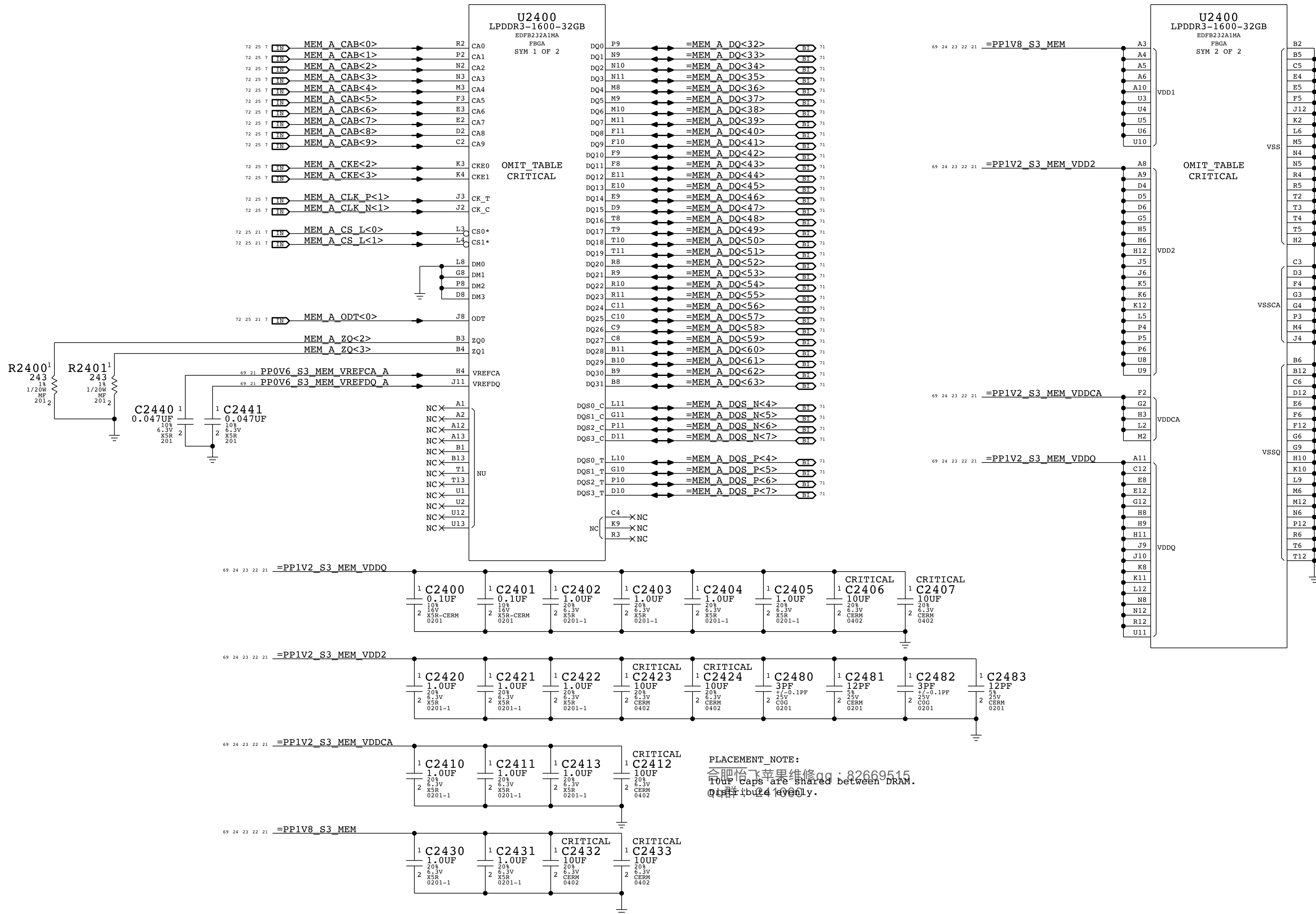
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	DRAWING NUMBER		SIZE
	051-02265		D
	REVISION		
	1.0.0		
	BRANCH		
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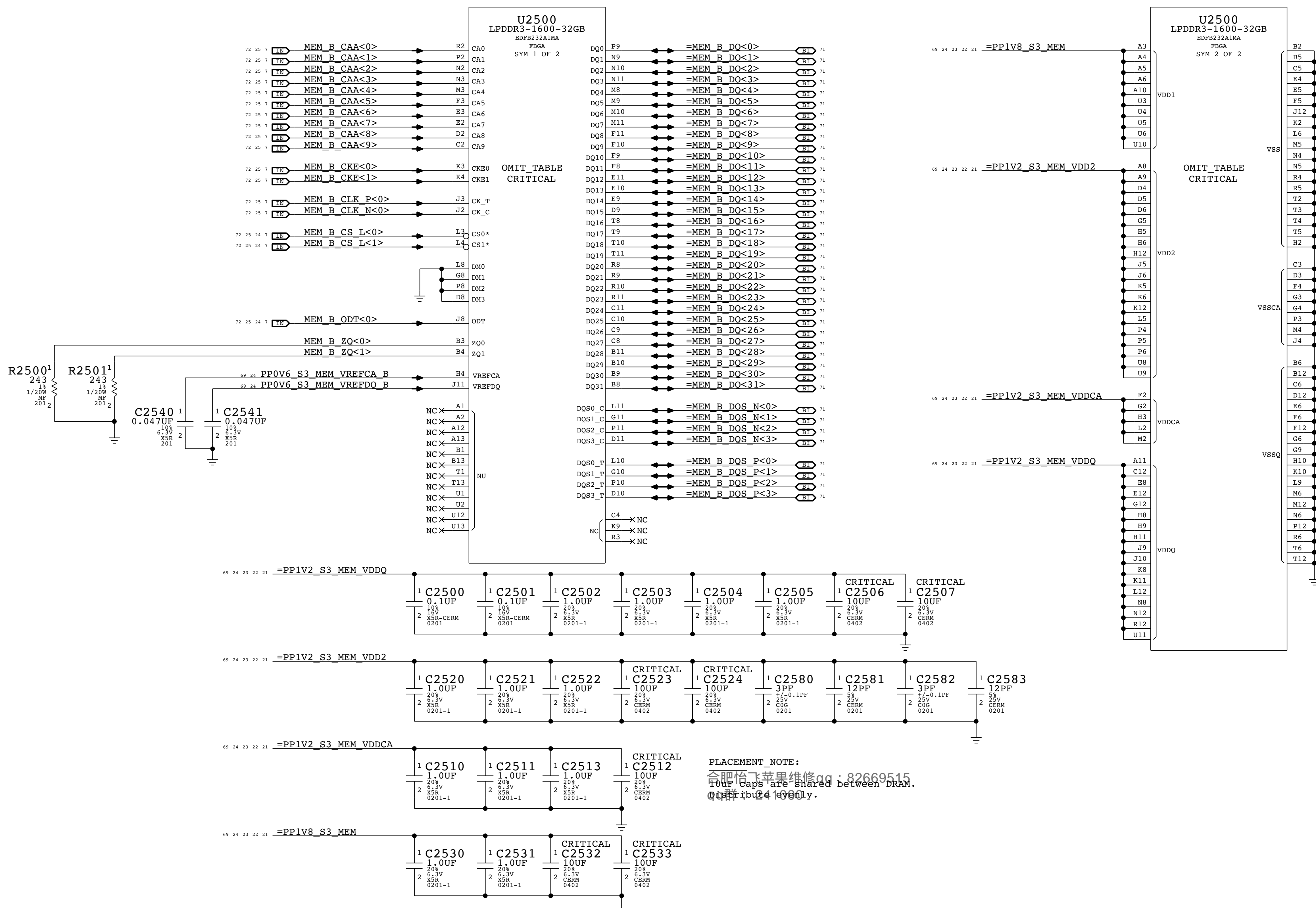
# LPDDR3 CHANNEL A (0-31)



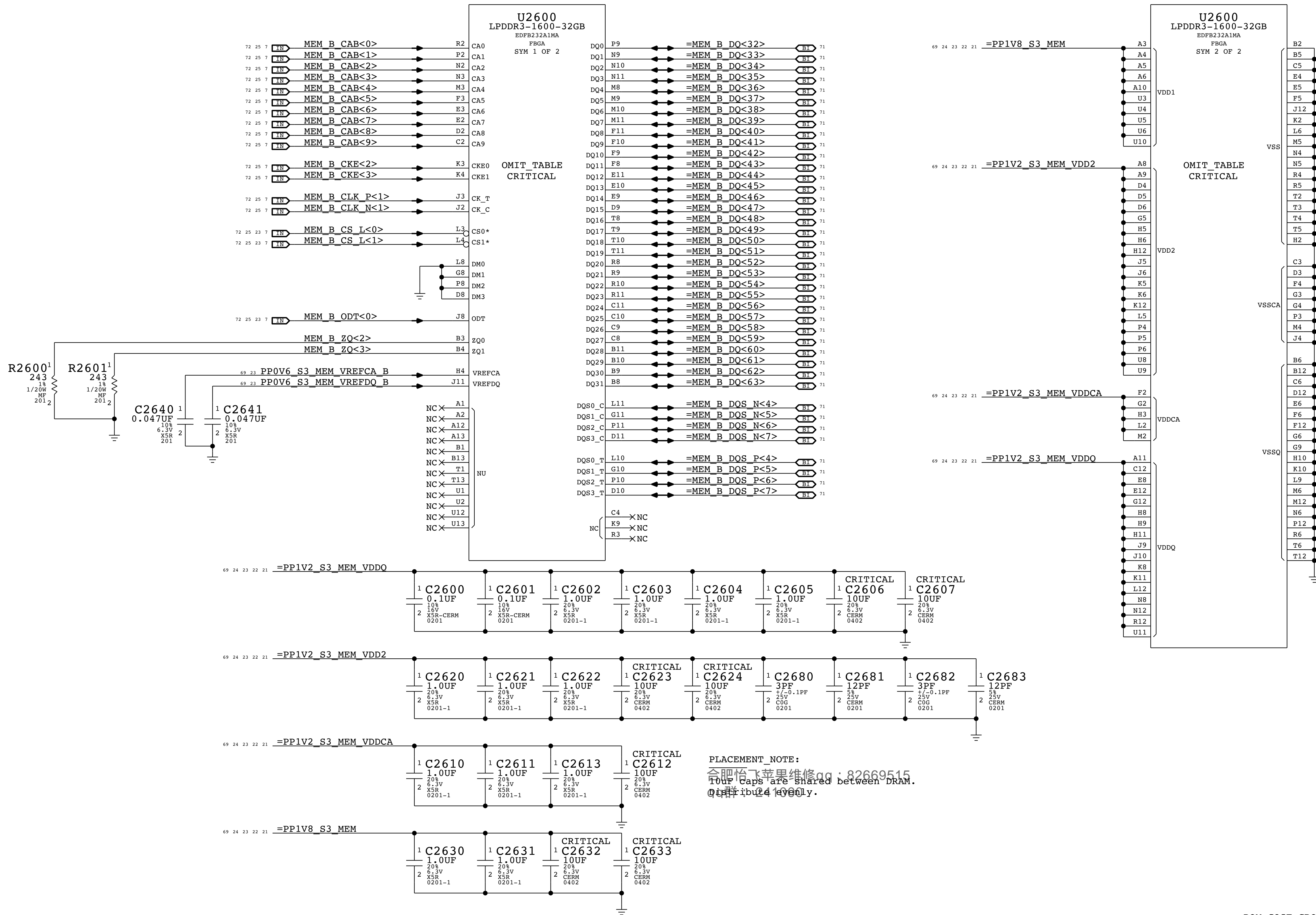
# LPDDR3 CHANNEL A (32-63)



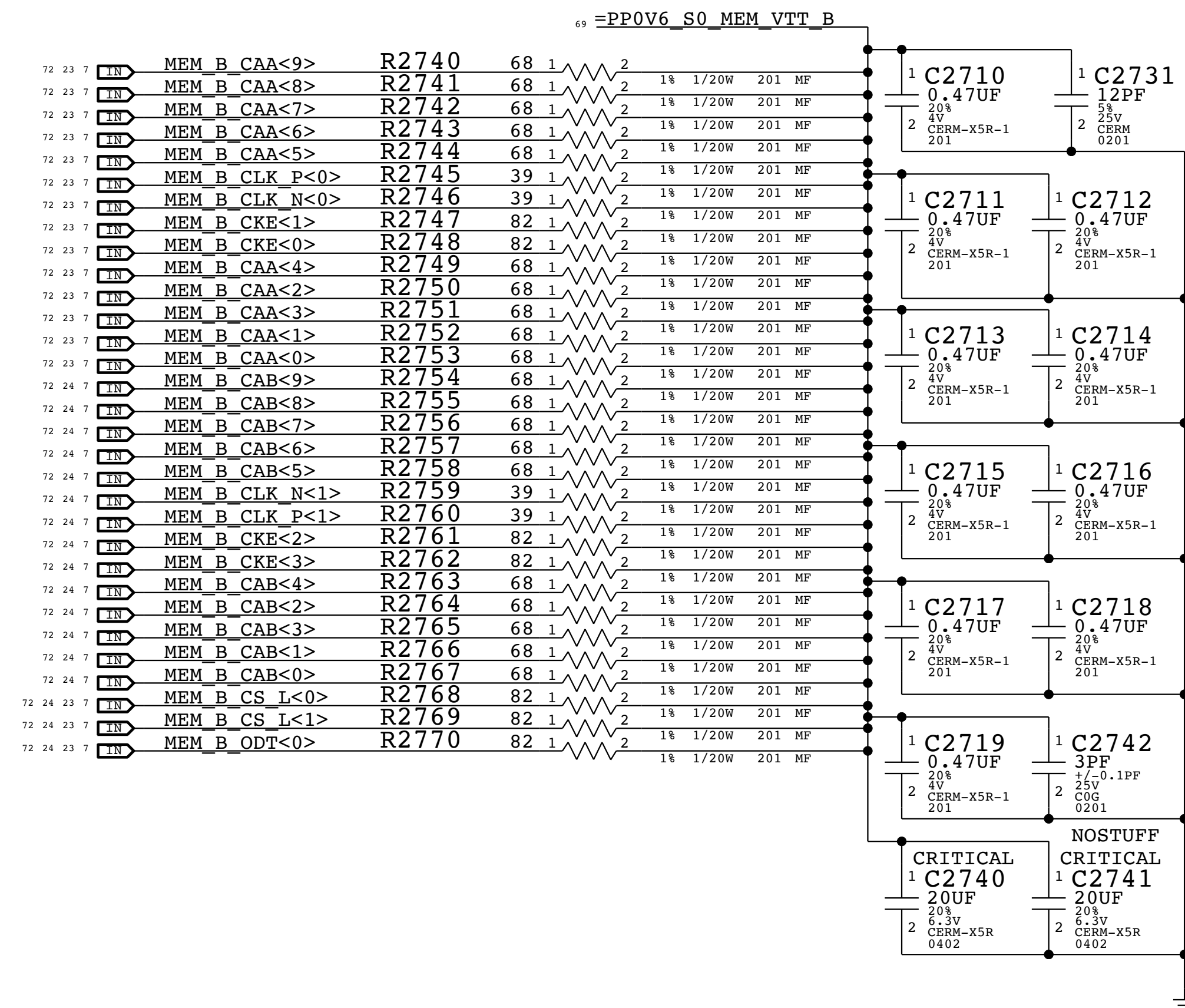
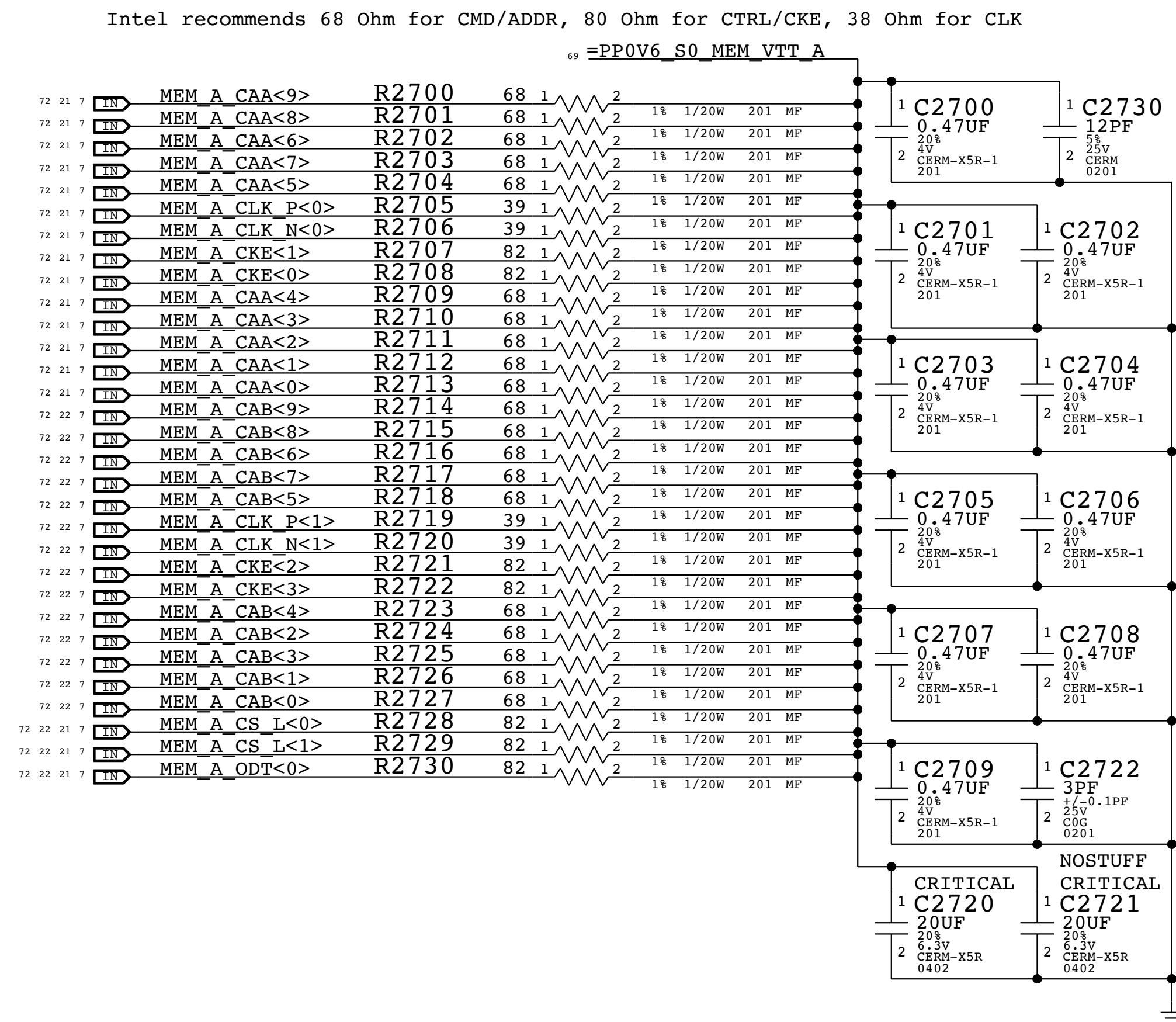
LPDDR3 CHANNEL B (0-31)




LPDDR3 CHANNEL B (32-63)





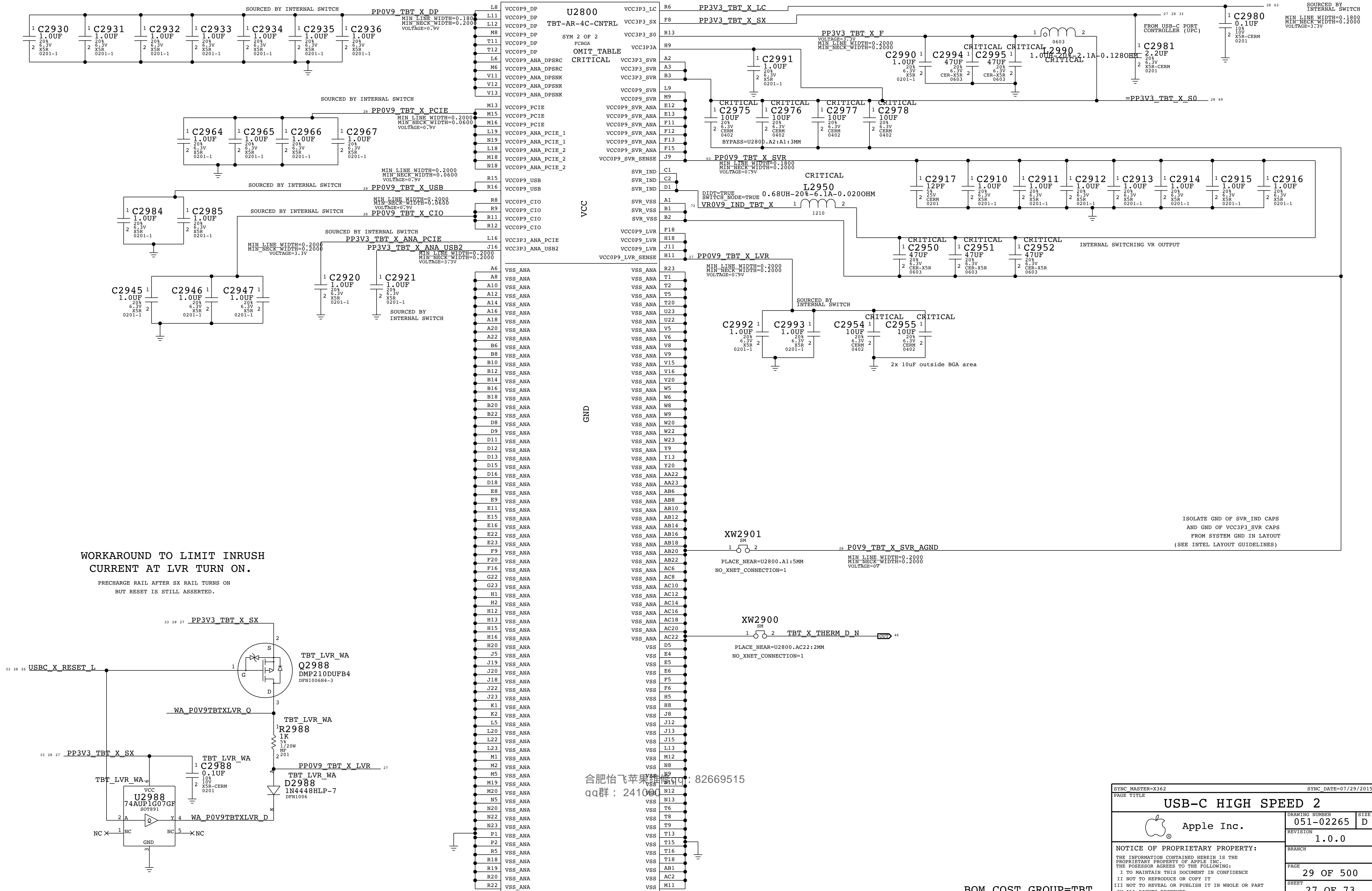


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SYNC MASTER=X502-EXP		SYNC DATE=12/03/2015	
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	Apple Inc.		DRAWING NUMBER 051-02265
			SIZE D
		REVISION 1.0.0	
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		SHEET 25 OF 73	

BOM\_COST\_GROUP=DRAM







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A

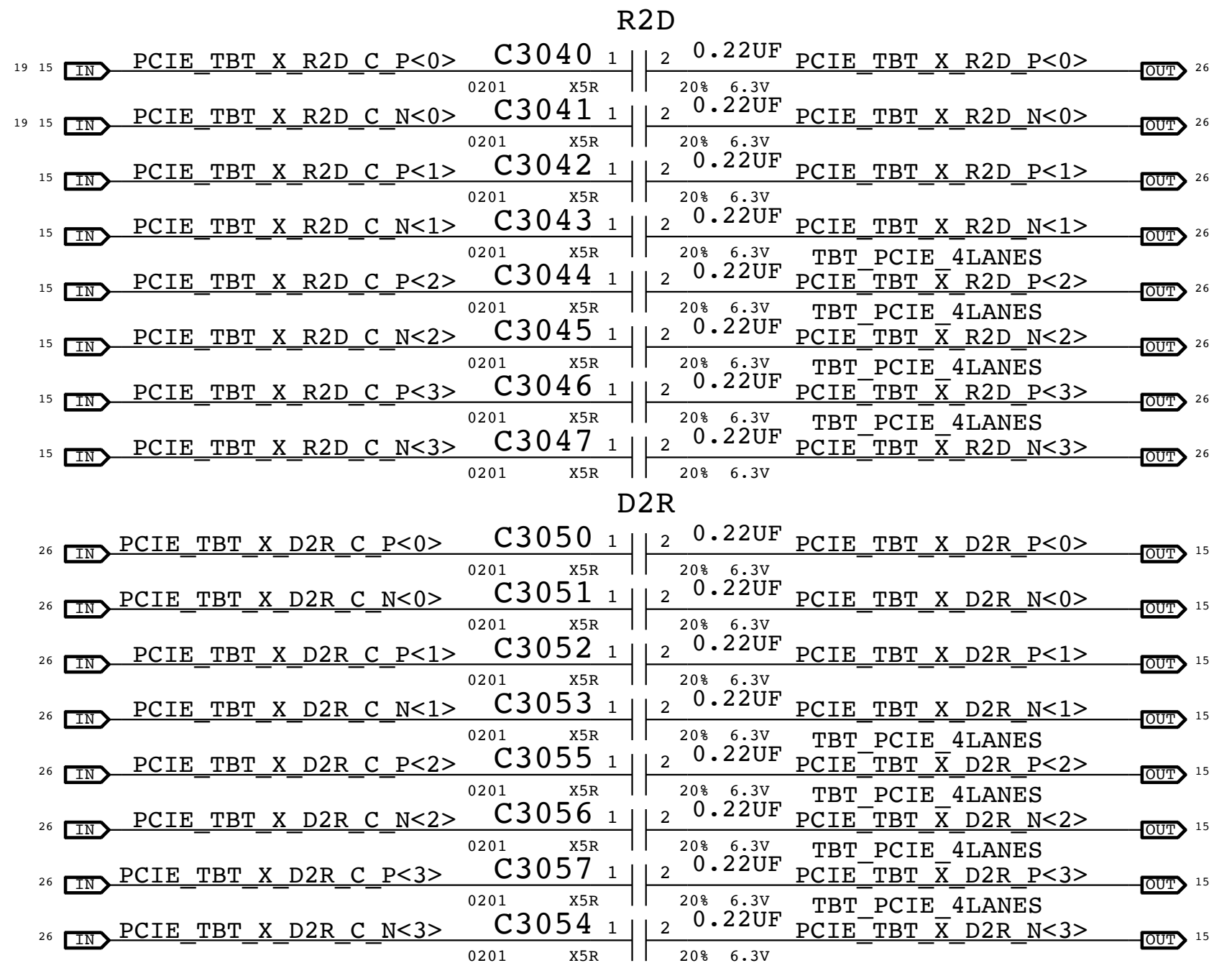
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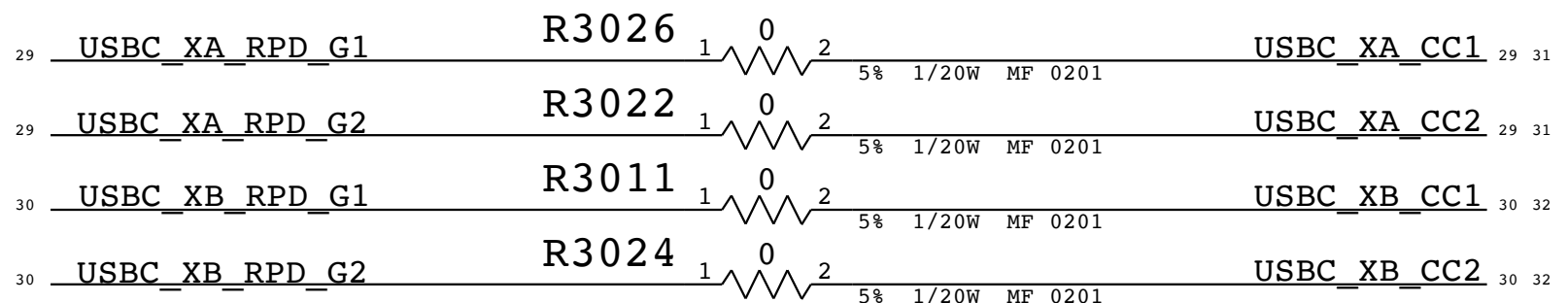
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RIDGE AC COUPLING

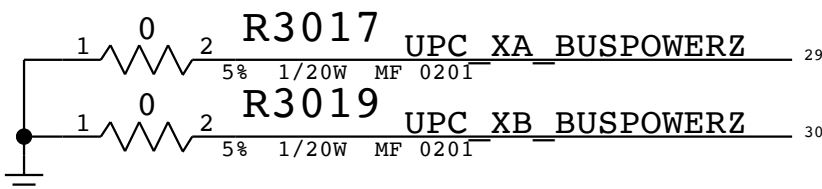


ACE RPD STRAPPING

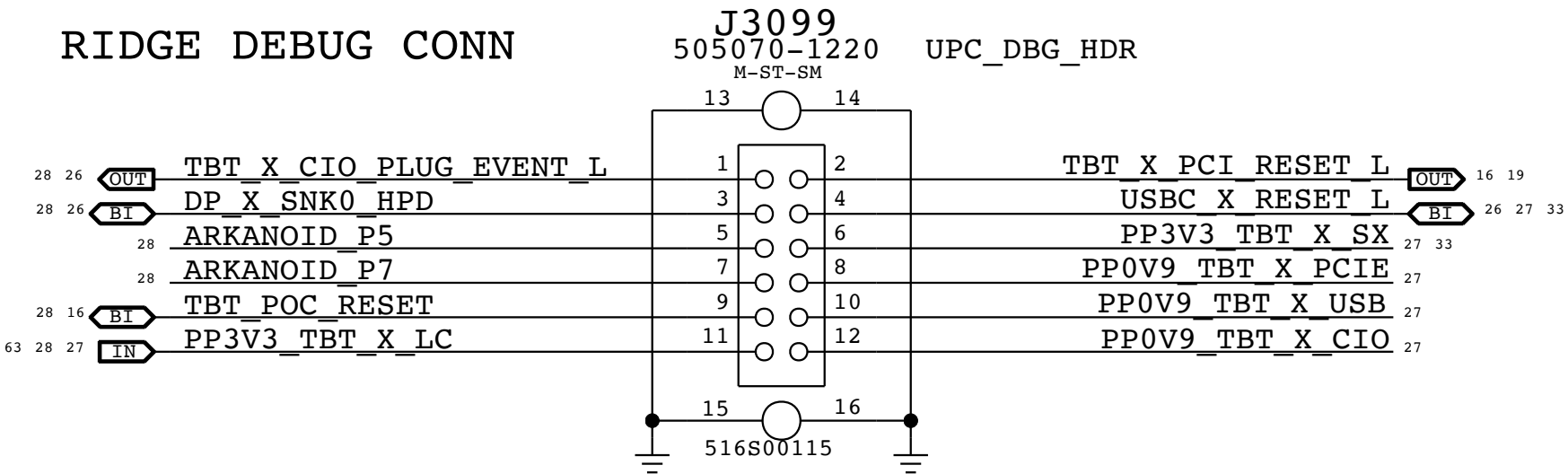
CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE  
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE



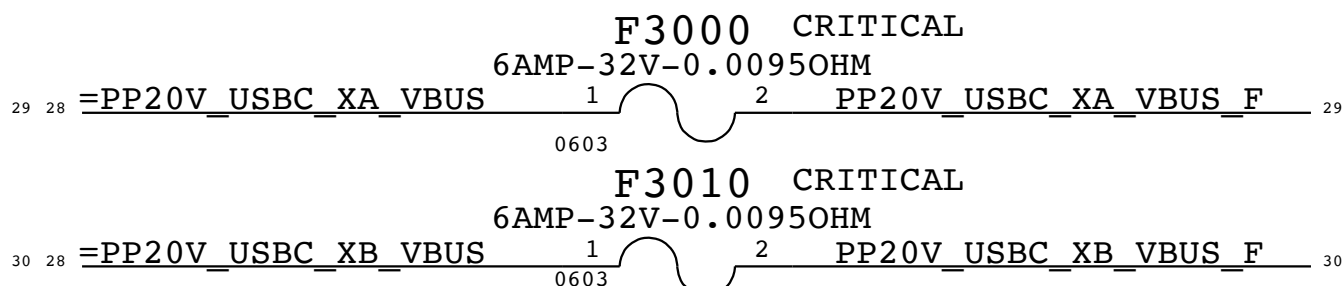
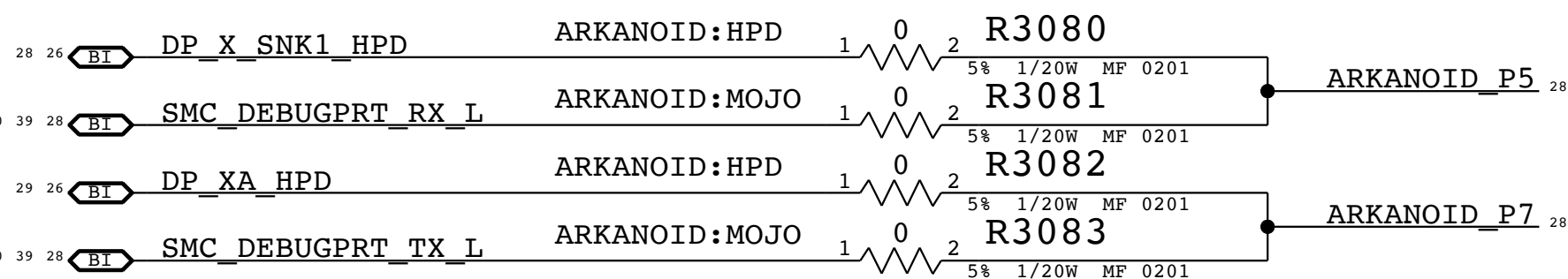
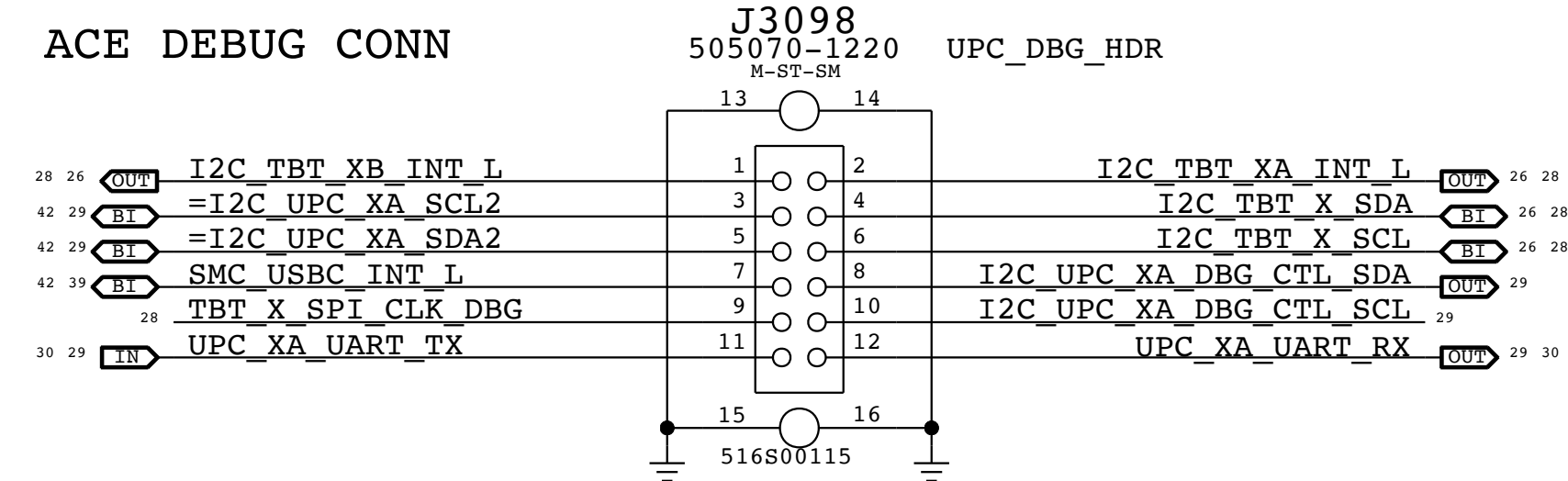
ACE BUSPOWERZ STRAPPING



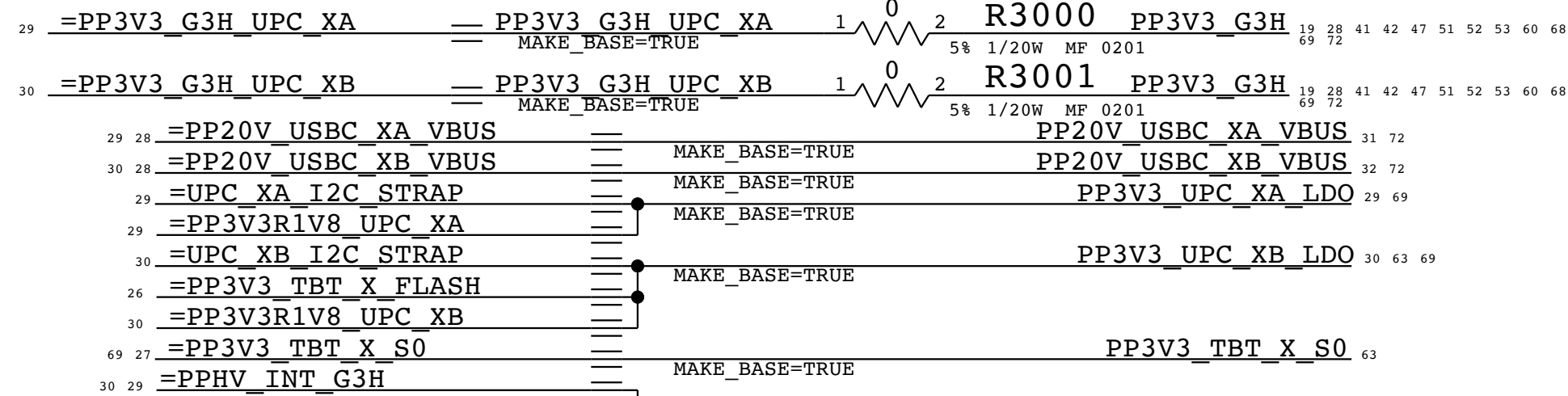
RIDGE DEBUG CONN



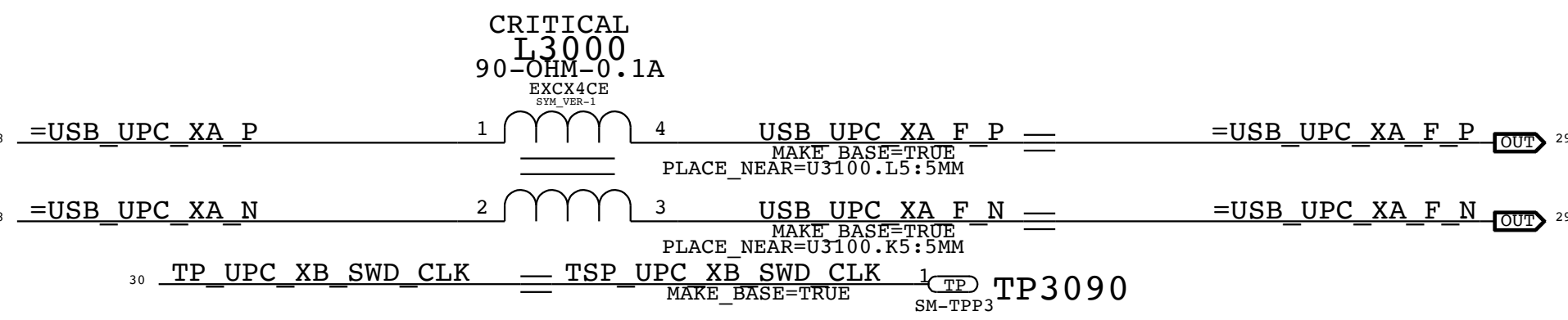
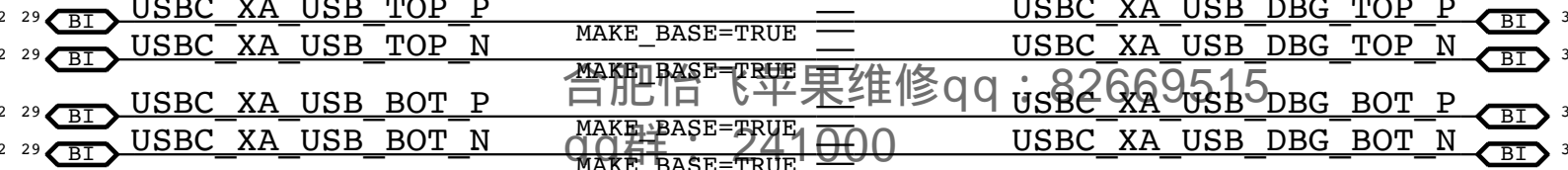
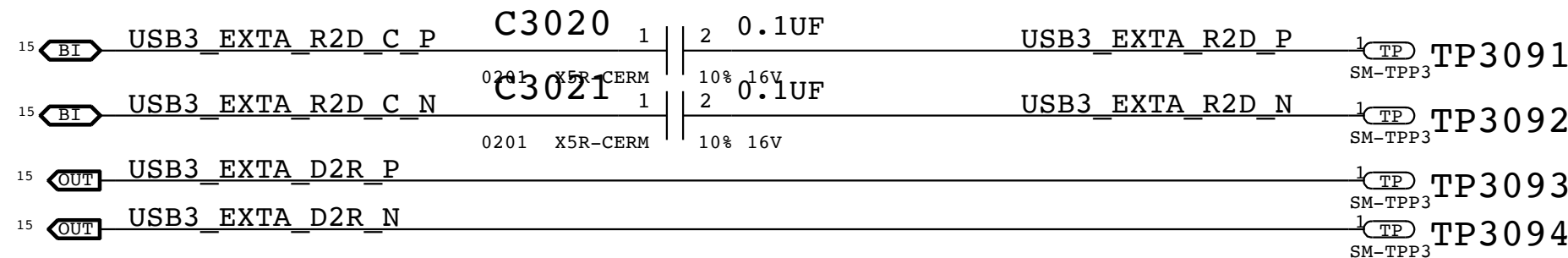
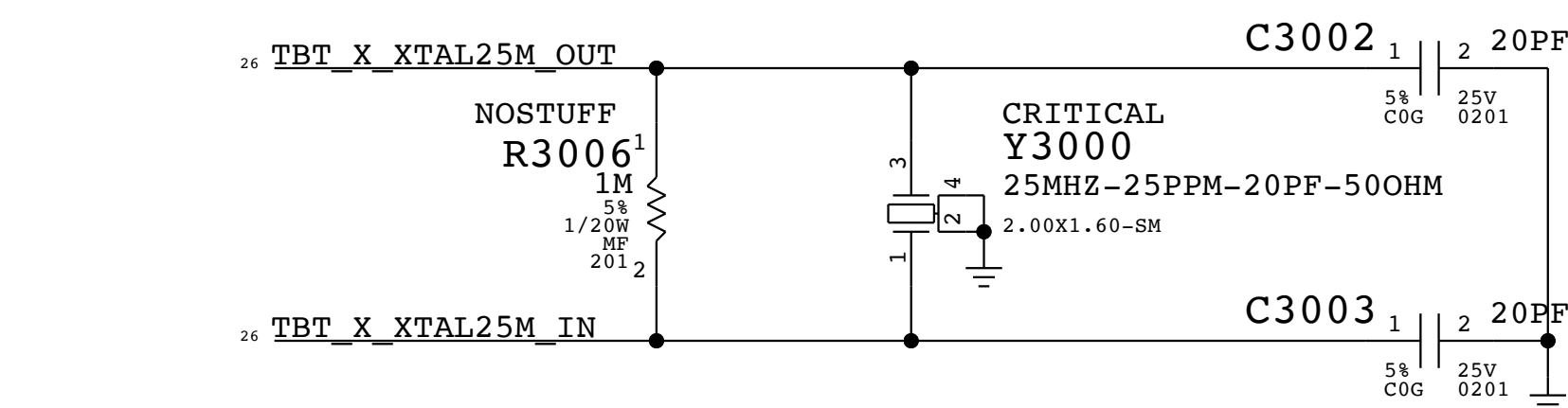
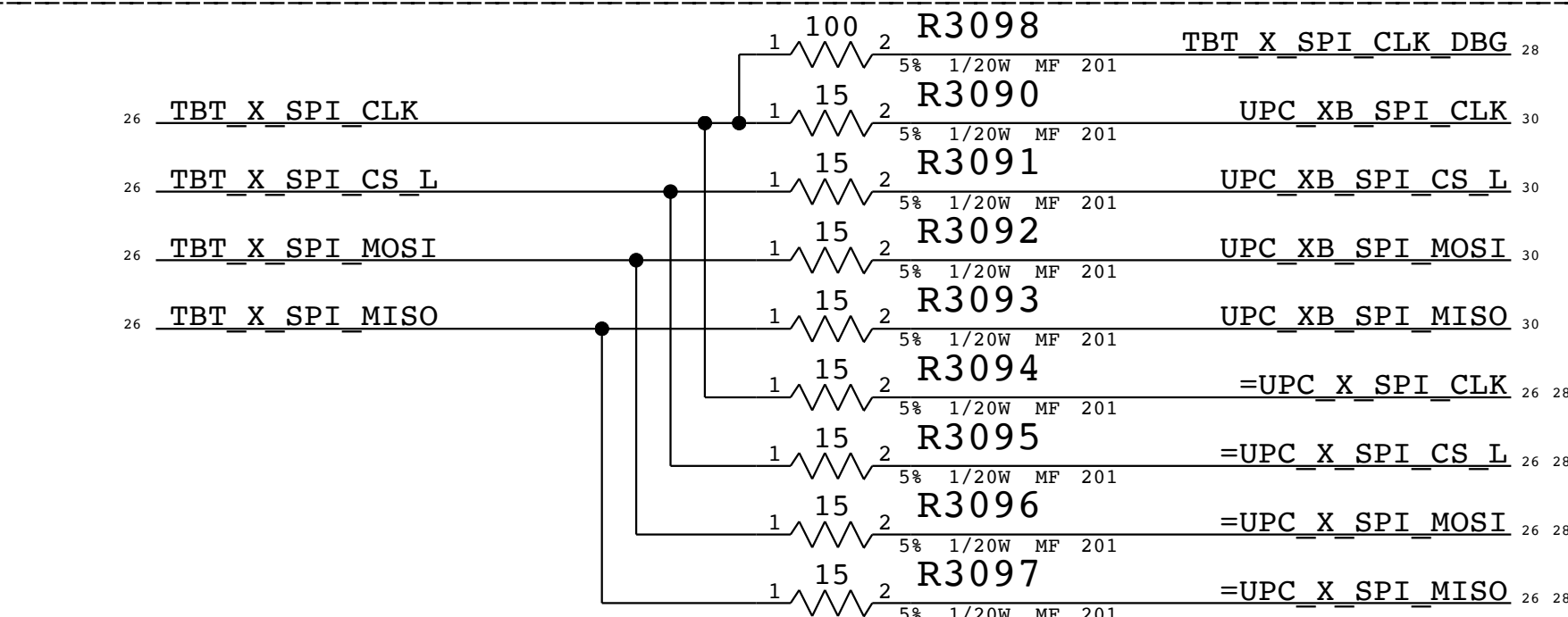
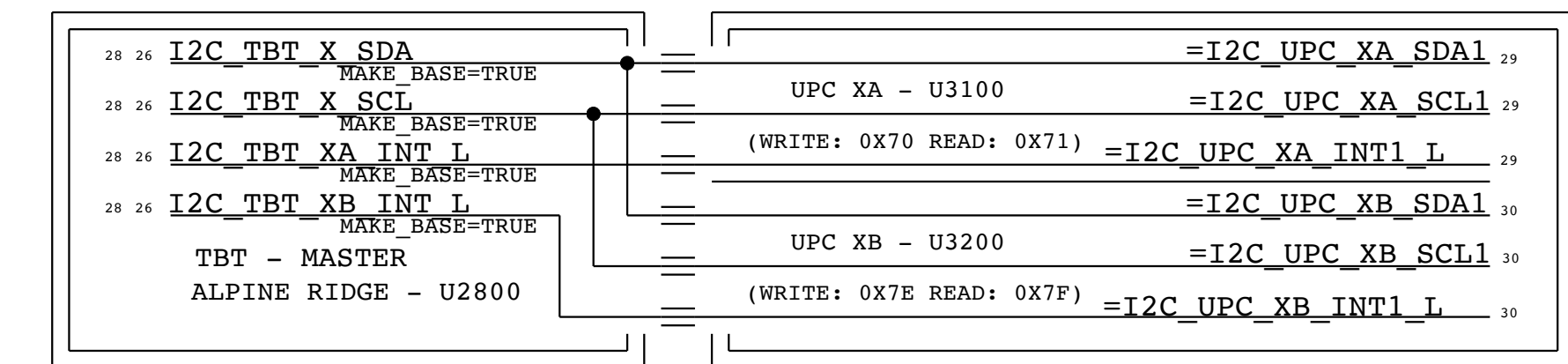
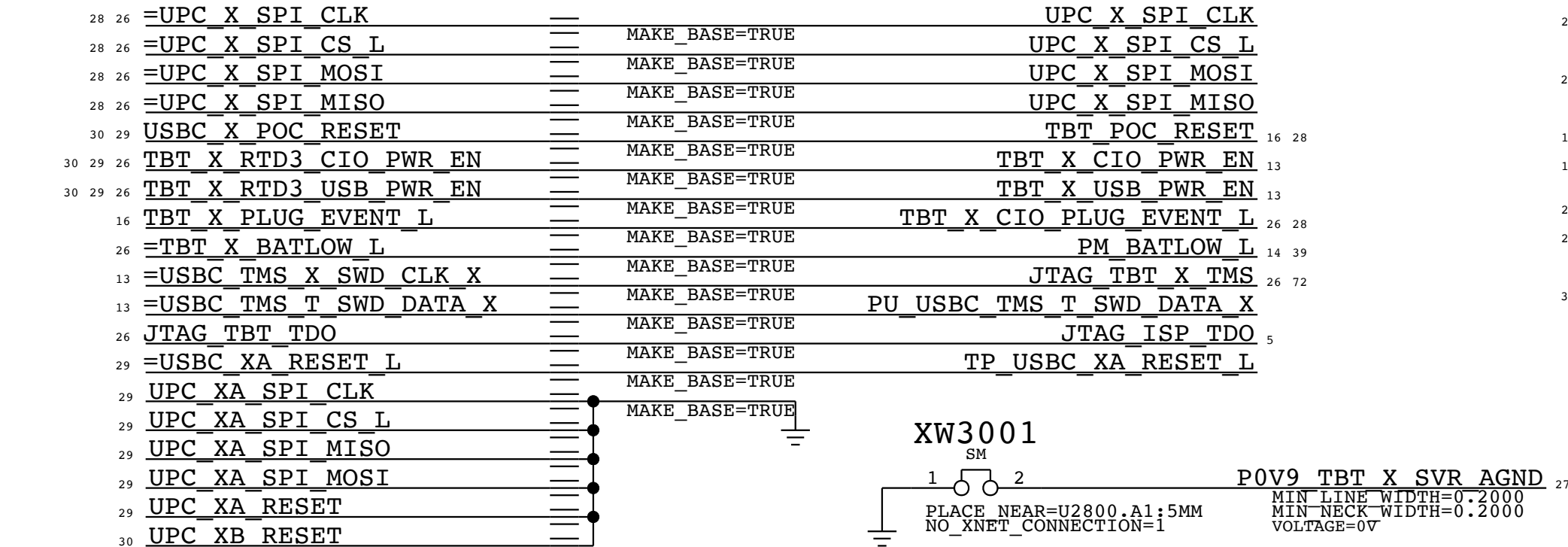
ACE DEBUG CONN



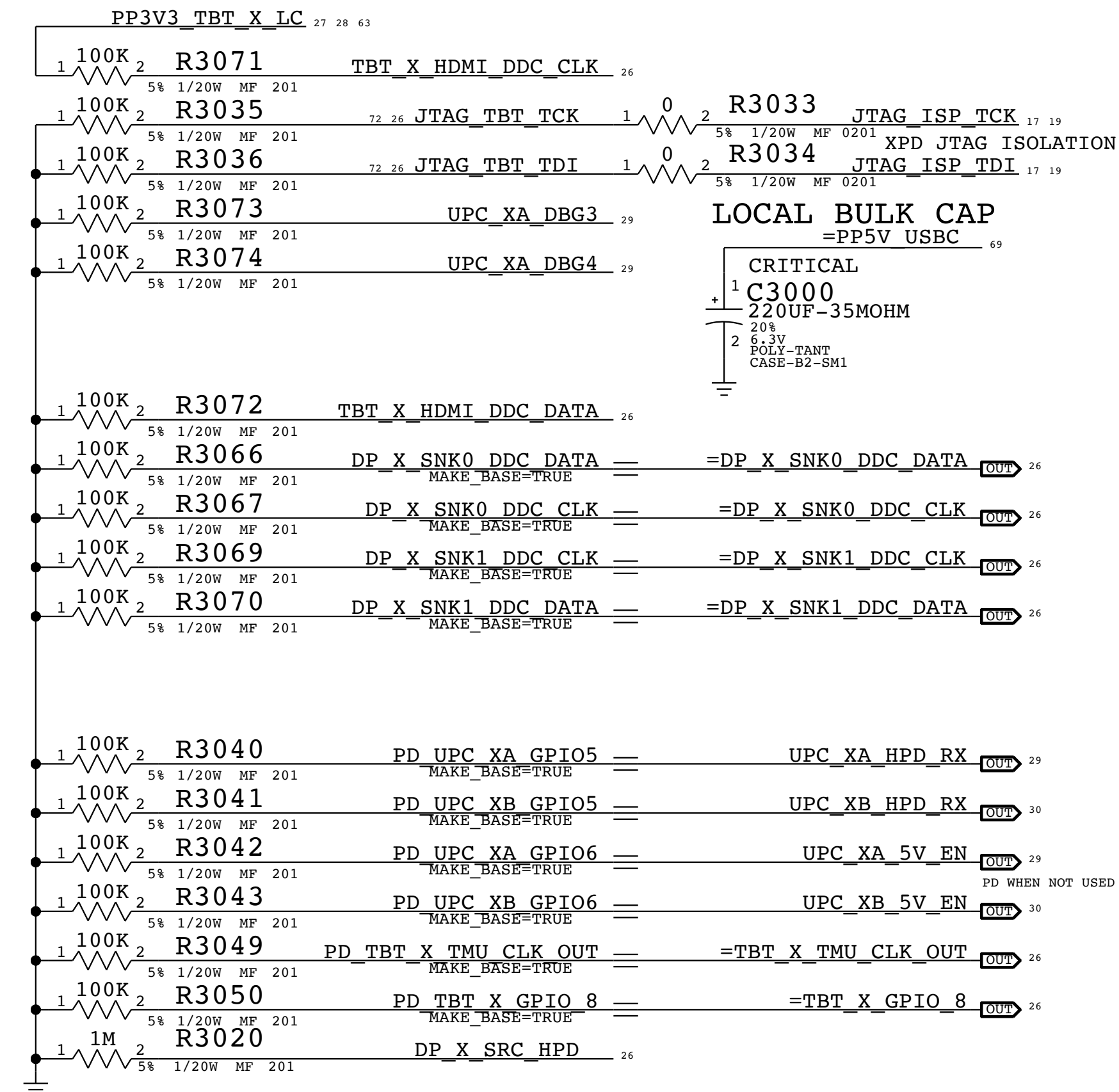
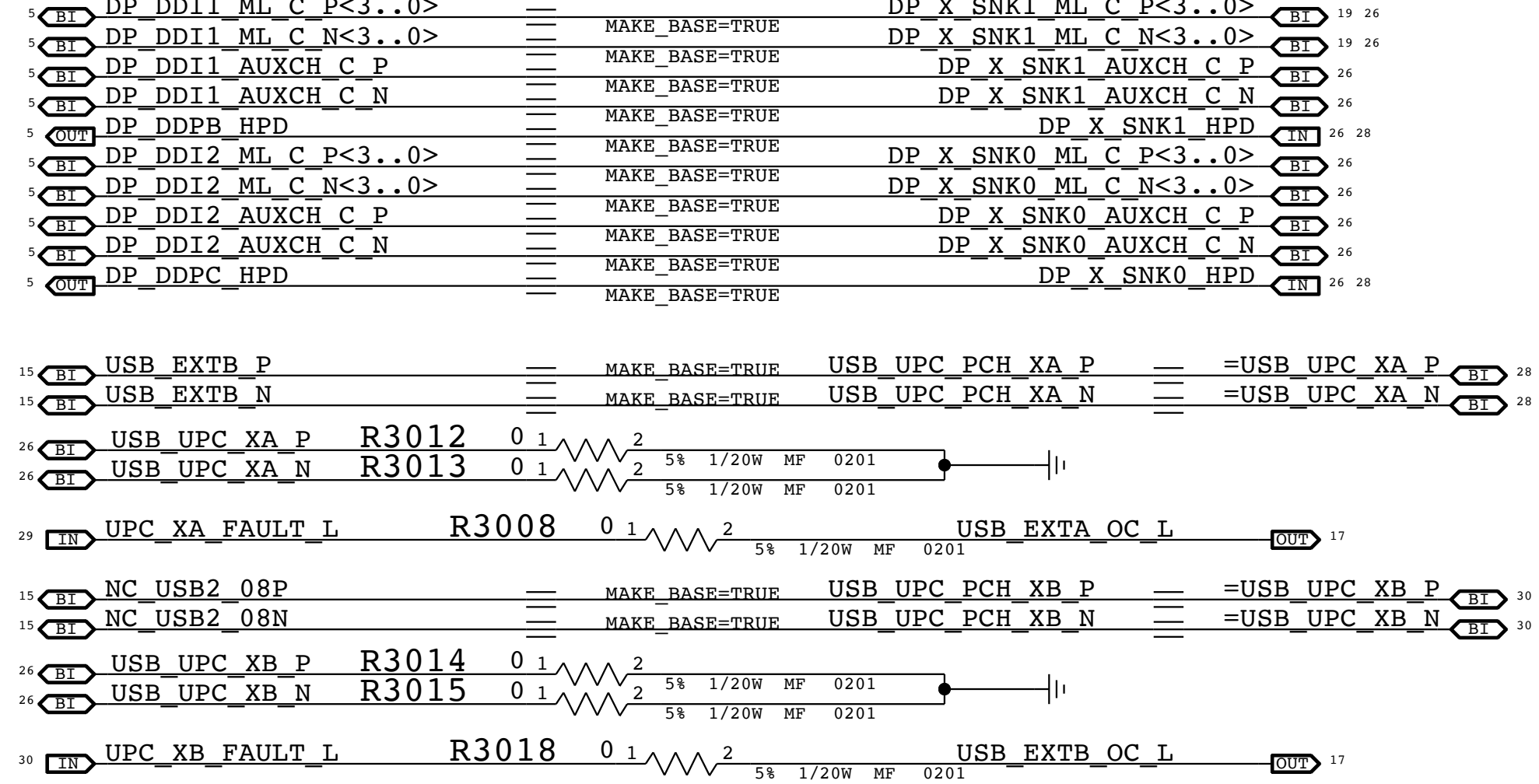
POWER ALIASES




MISC ALIASES



DP / USB SOURCE ALIASES



DESIGN: X502/MLB CATZ  
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE		
USB-C SUPPORT		
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BOM\_COST\_GROUP=USB-C

## D

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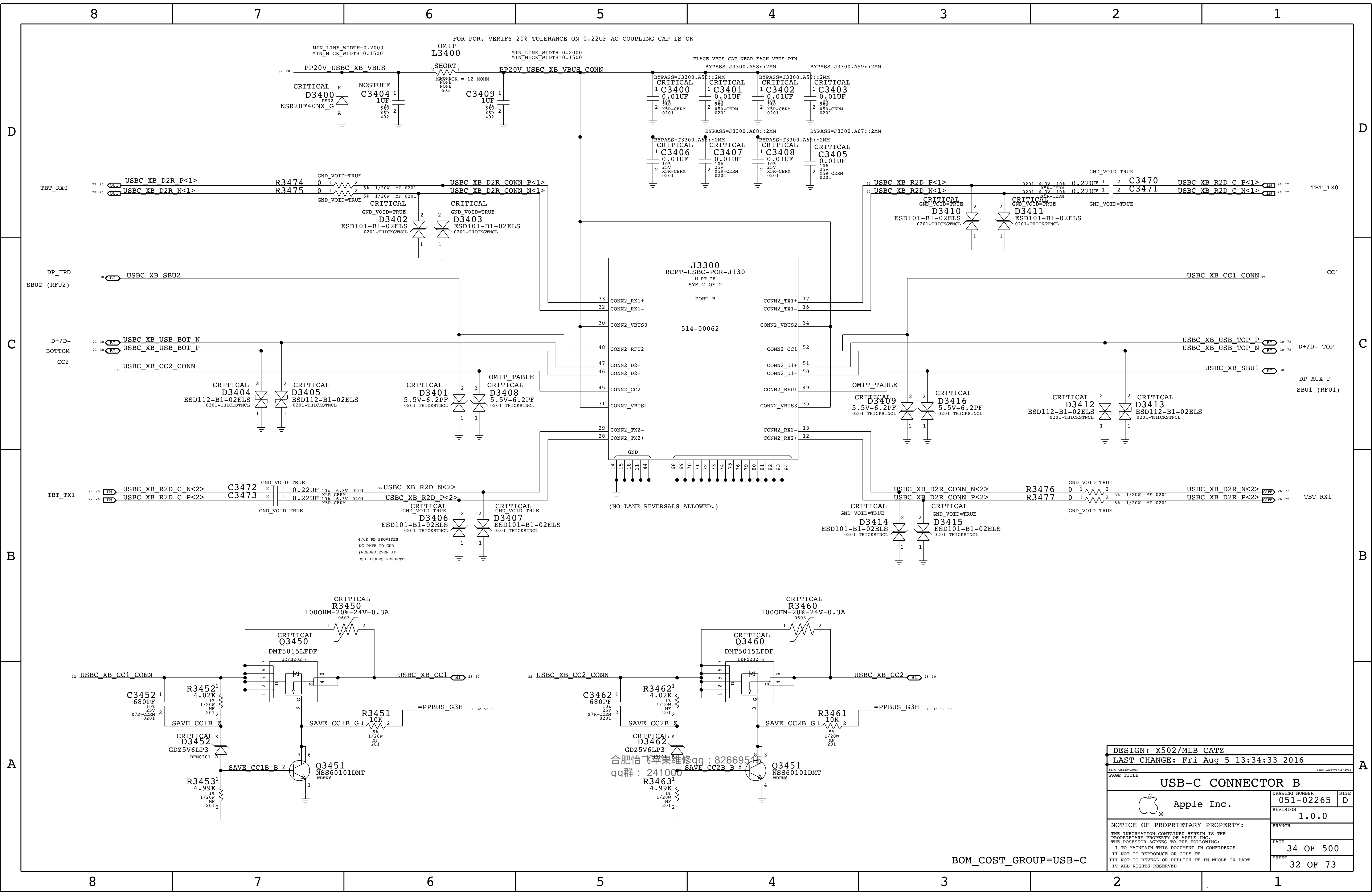
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BOM COST GROUP=USB-C





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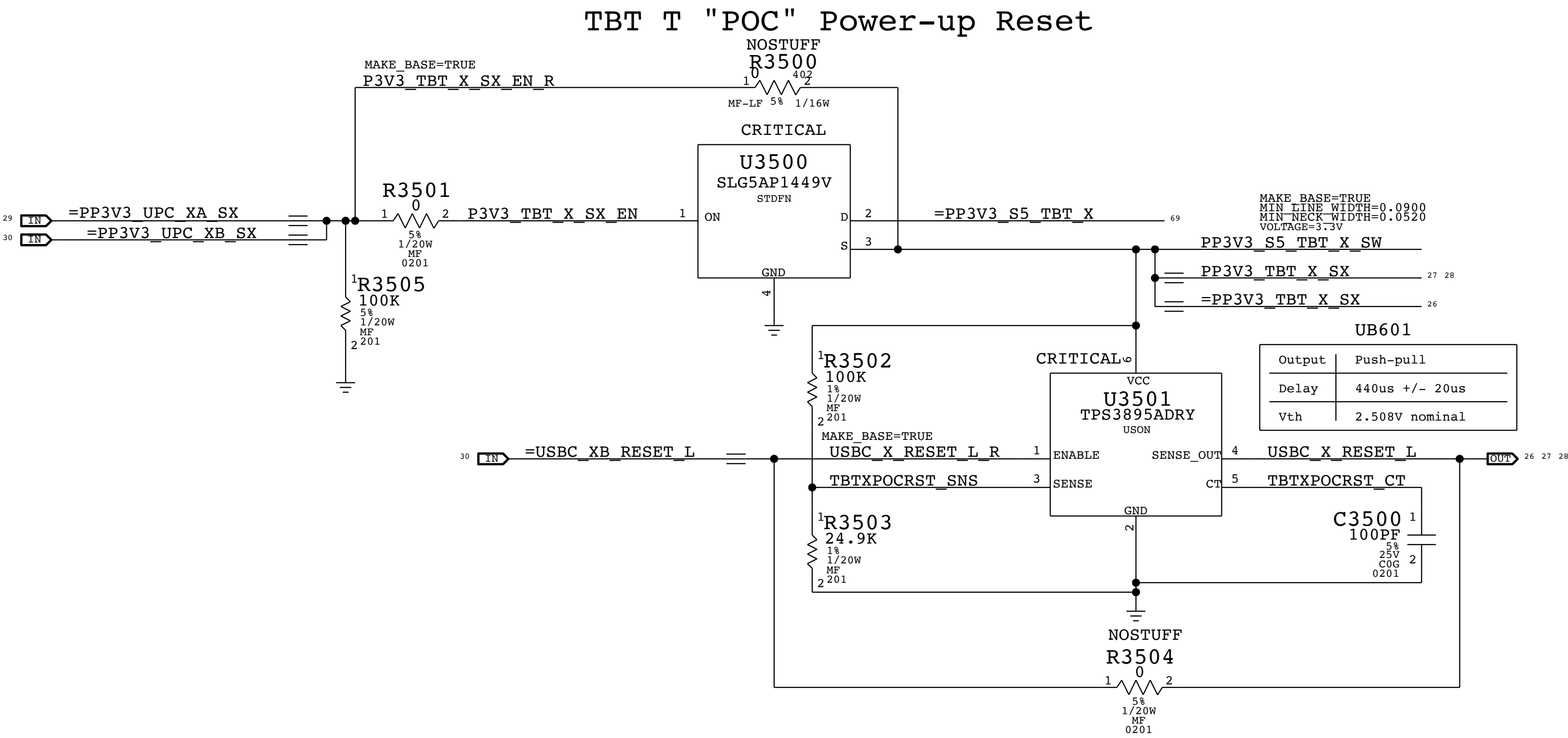
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BOM\_COST\_GROUP=USB-C

DESIGN: X502/MLB CATZ		
LAST CHANGE: Thu Aug 4 21:00:42 2016		
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USB-C SUPPORT 2		
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	SHEET	33 OF 73

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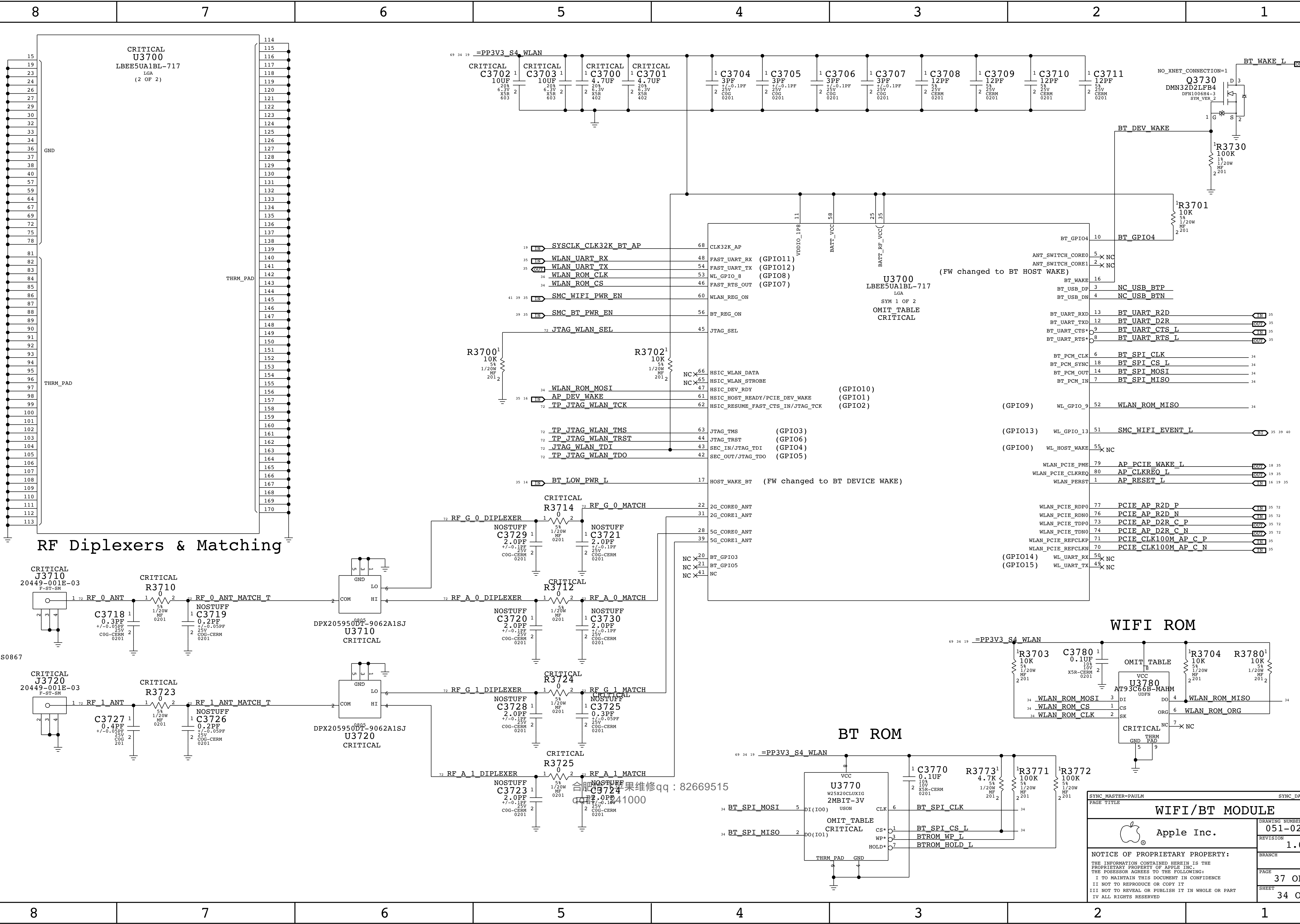
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### RF Diplexers & Matching

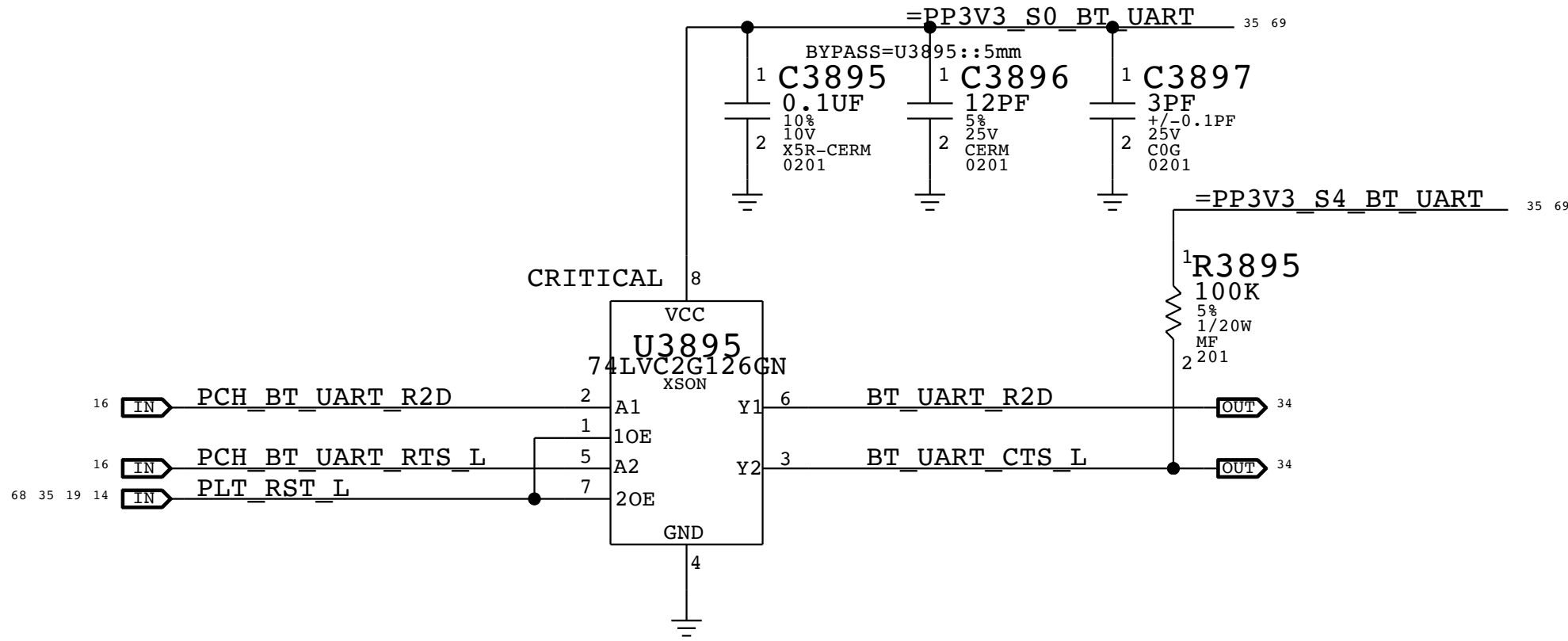
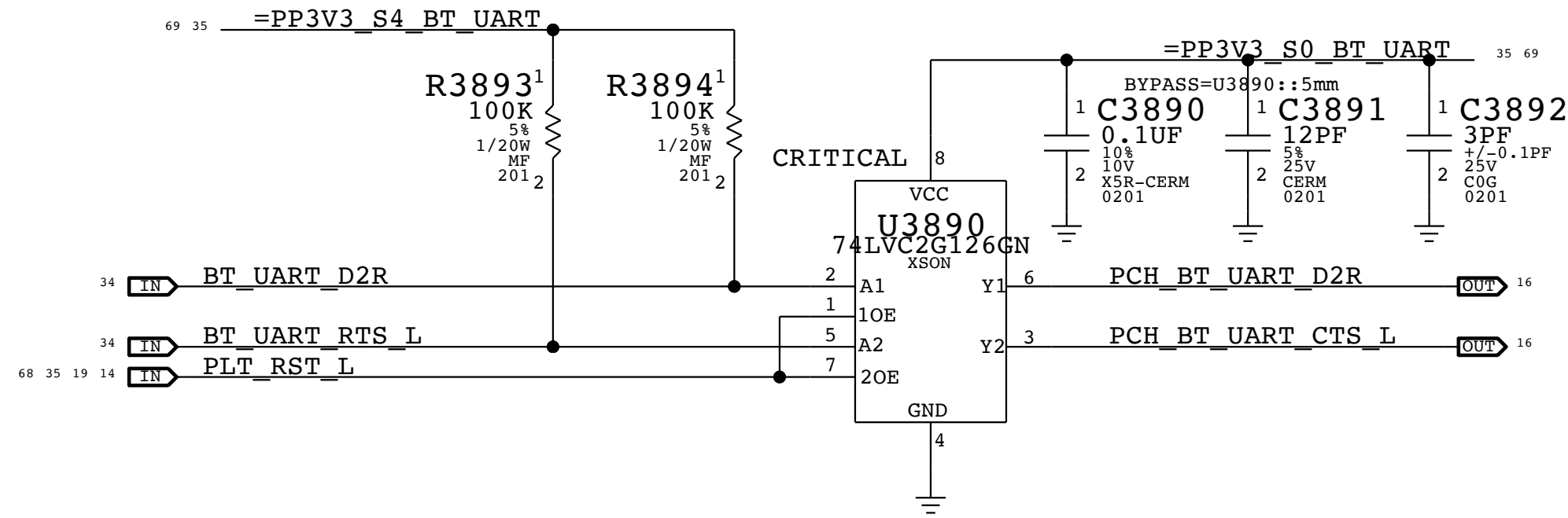
### WIFI ROM

### BT ROM

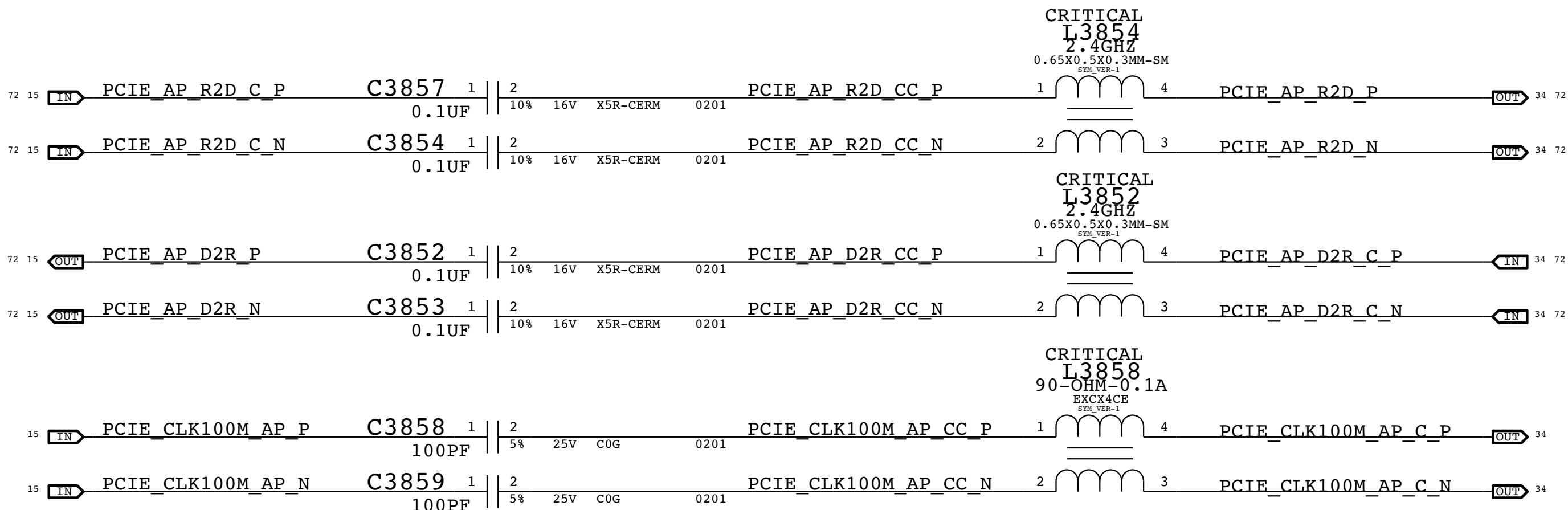
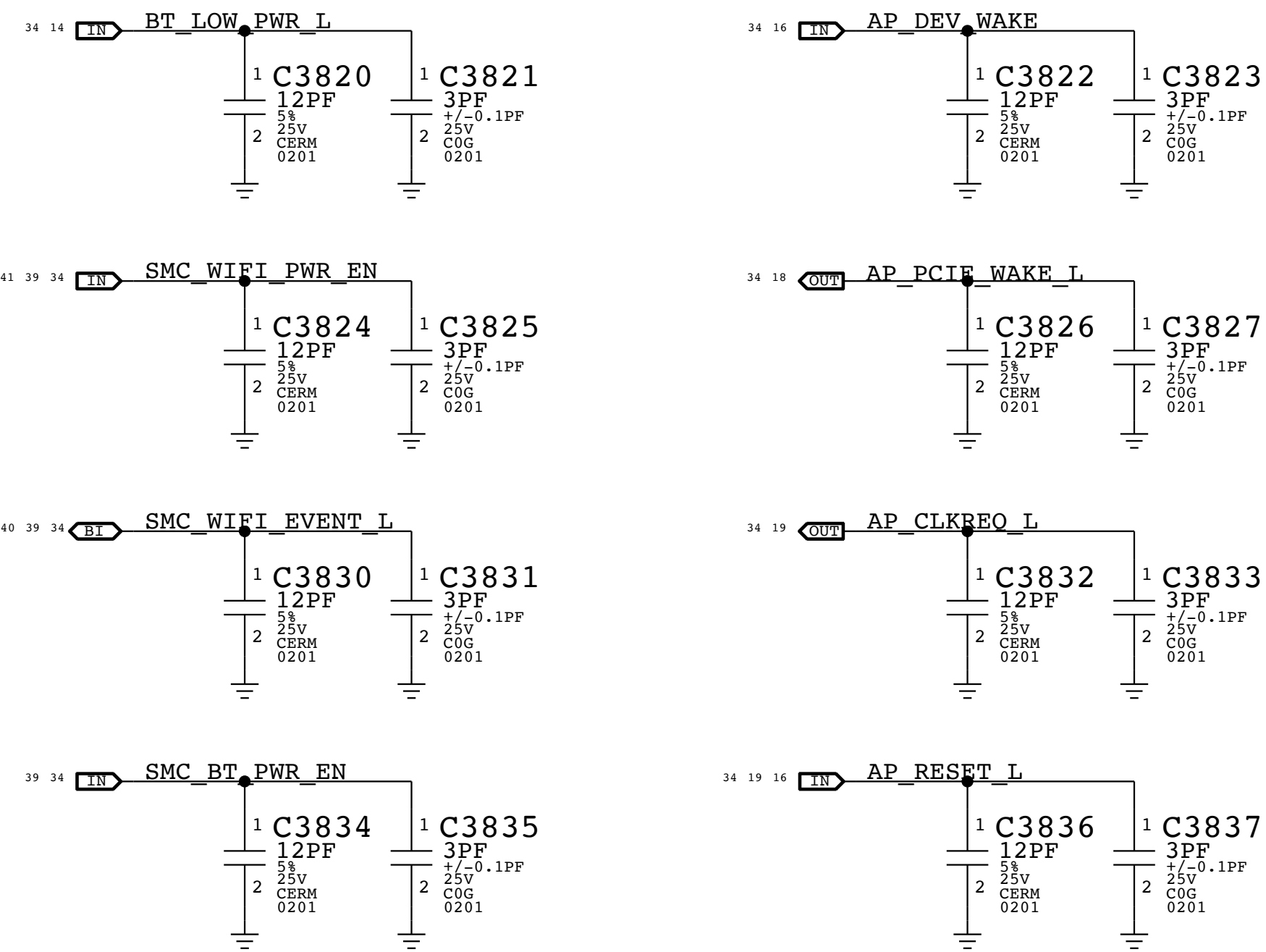
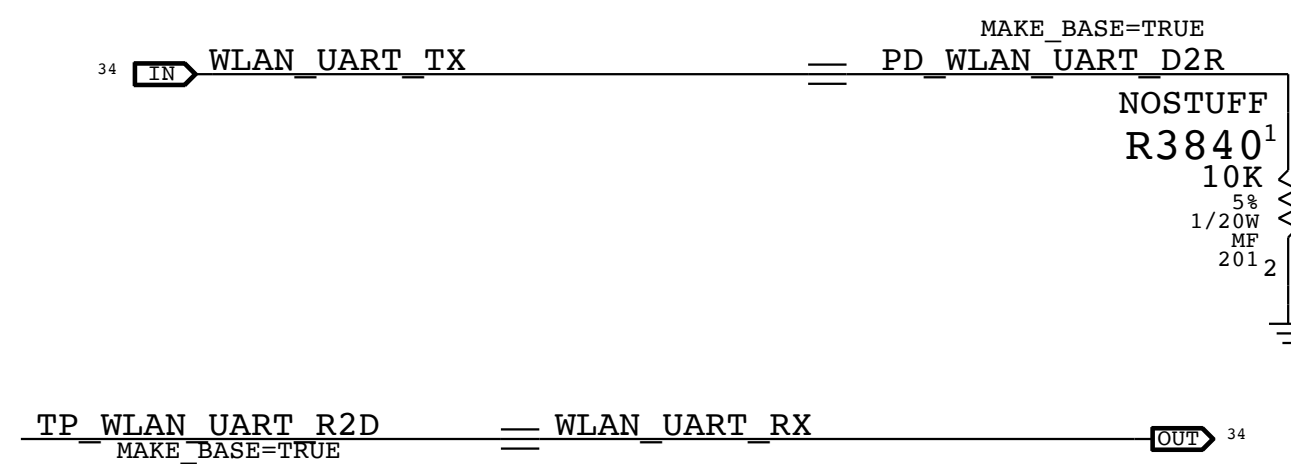
SYNC MASTER=PAULM		SYNC DATE=06/15/2015	
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WIFI/BT MODULE			
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		PAGE	37 OF 500
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BT UART Isolation

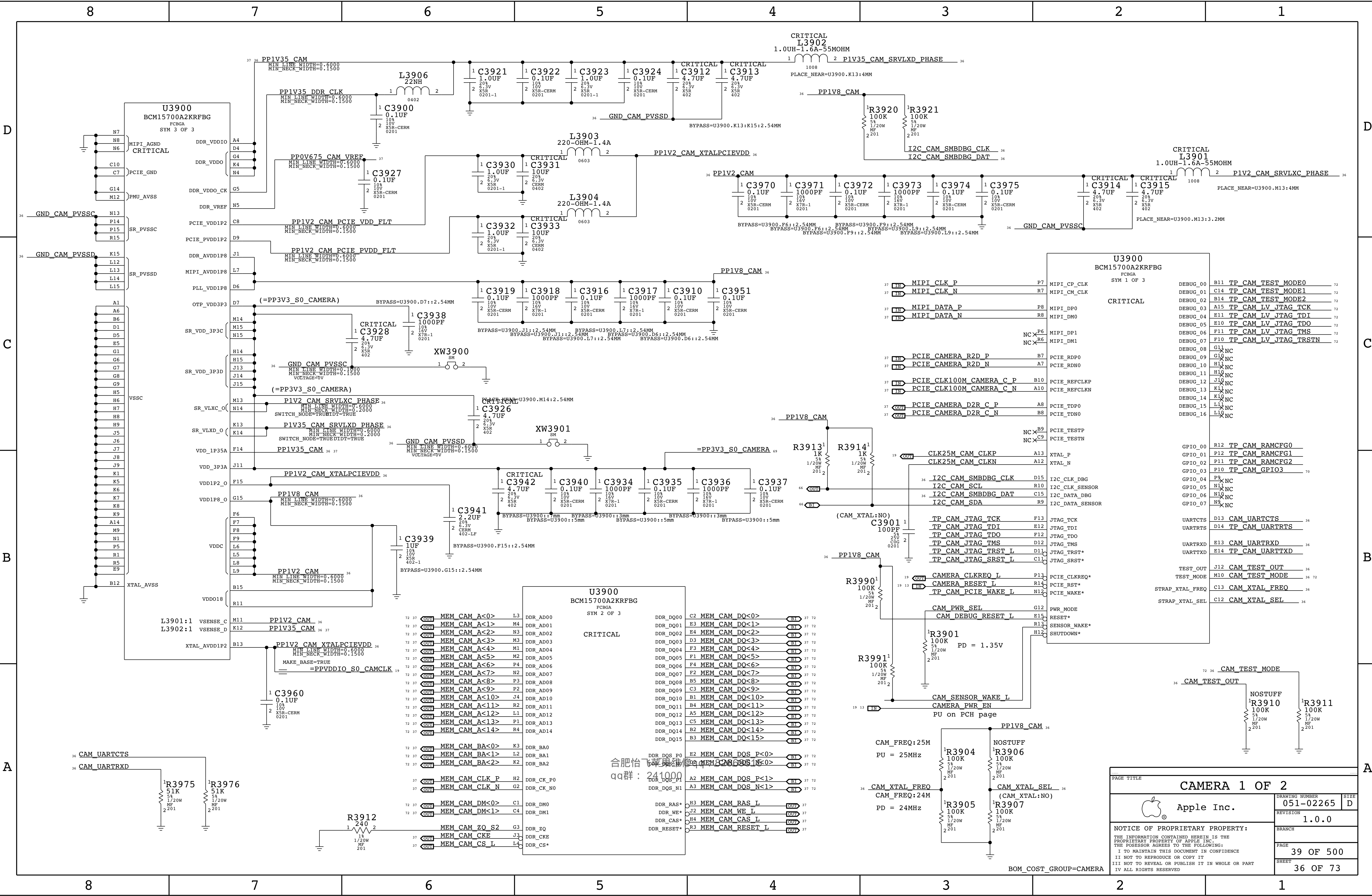


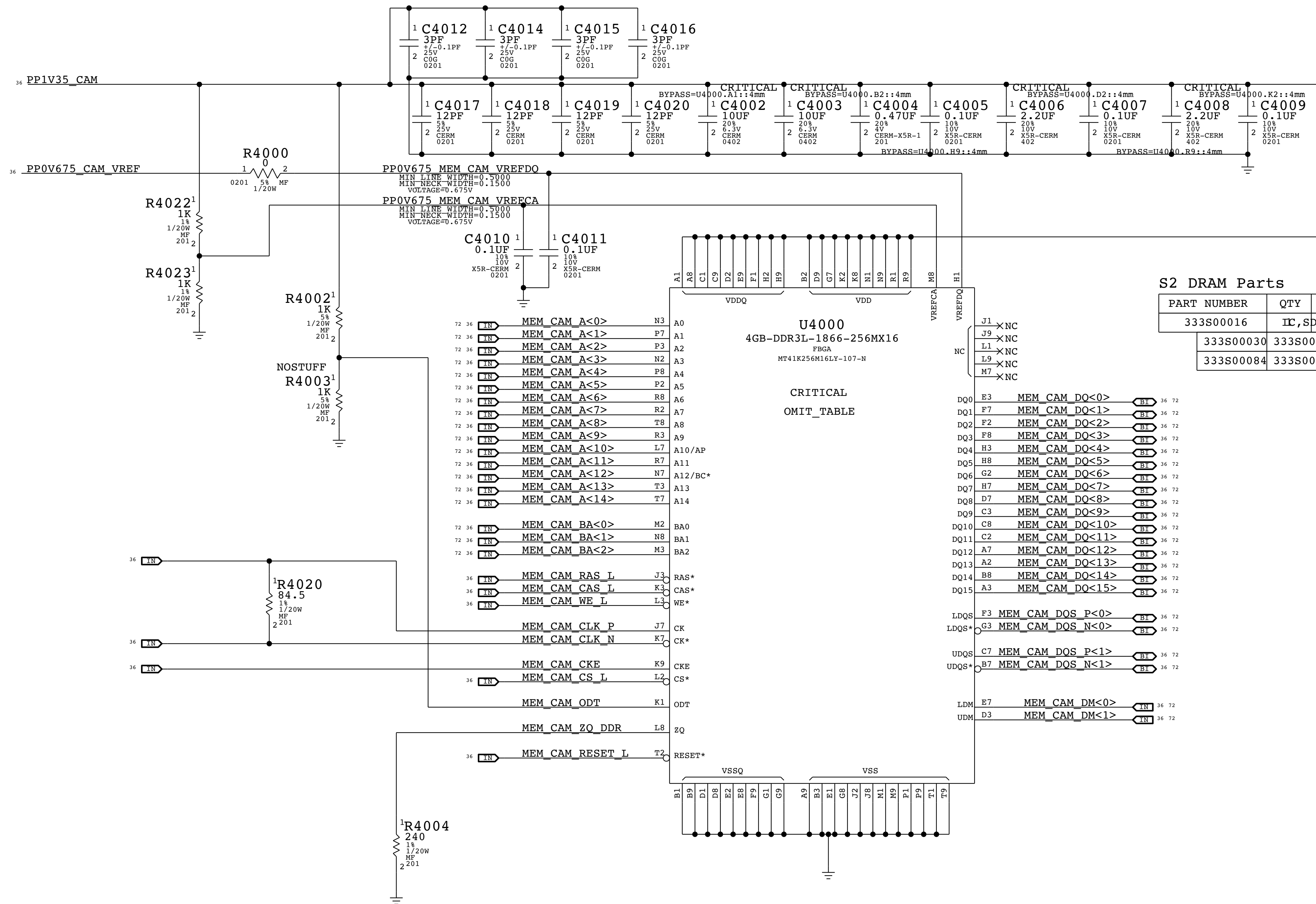
WIFI UART ISOLATION



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qq群 : 241000

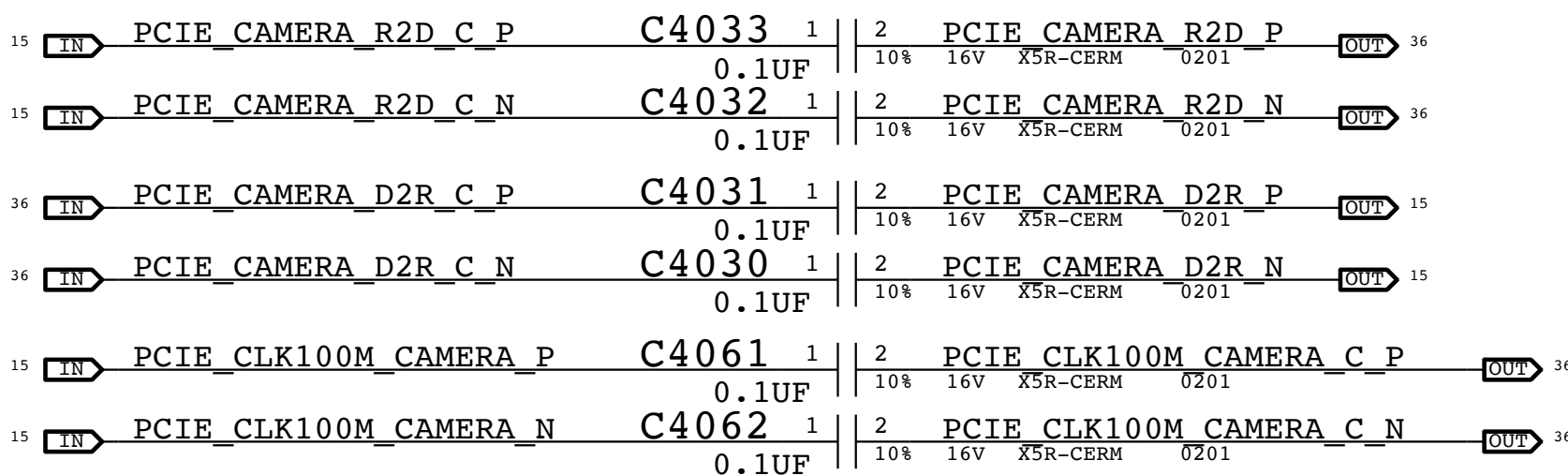
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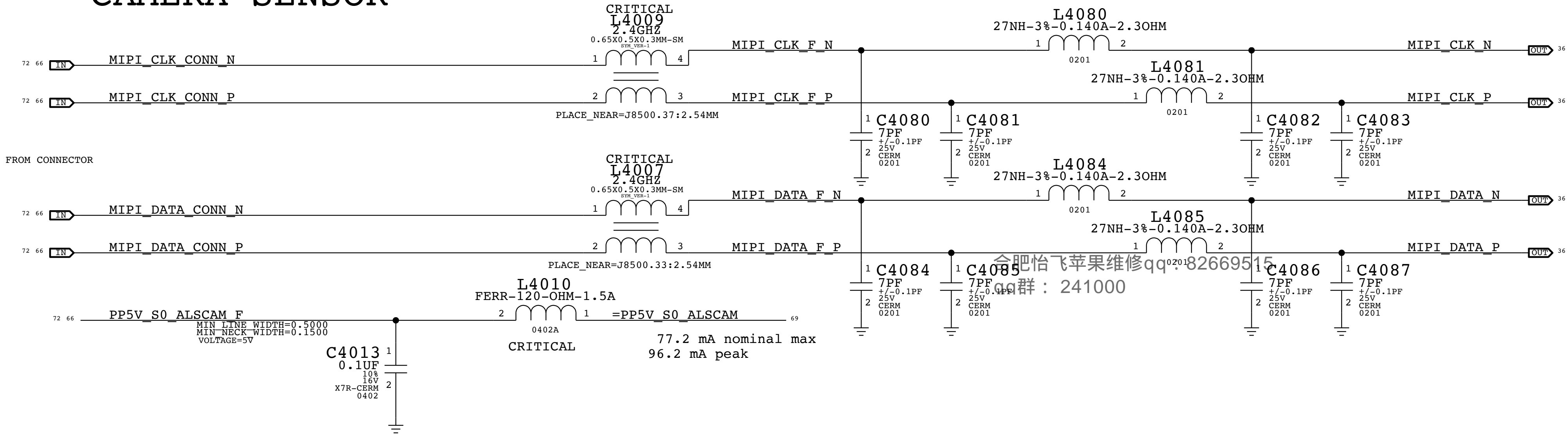


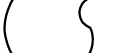
## S2 DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00016	1C	SDRAM, 25NM 4GB, DDR3L-1866, 96B	FBGA U4000	CRITICAL	
333S00030	333S00016		ALL		HYNIX ALT TO MICRON FOR S2 CAMERA DDR3 MEMORY
333S00084	333S00016		ALL		MICRON 20NM FOR S2 CAMERA DDR3 MEMORY



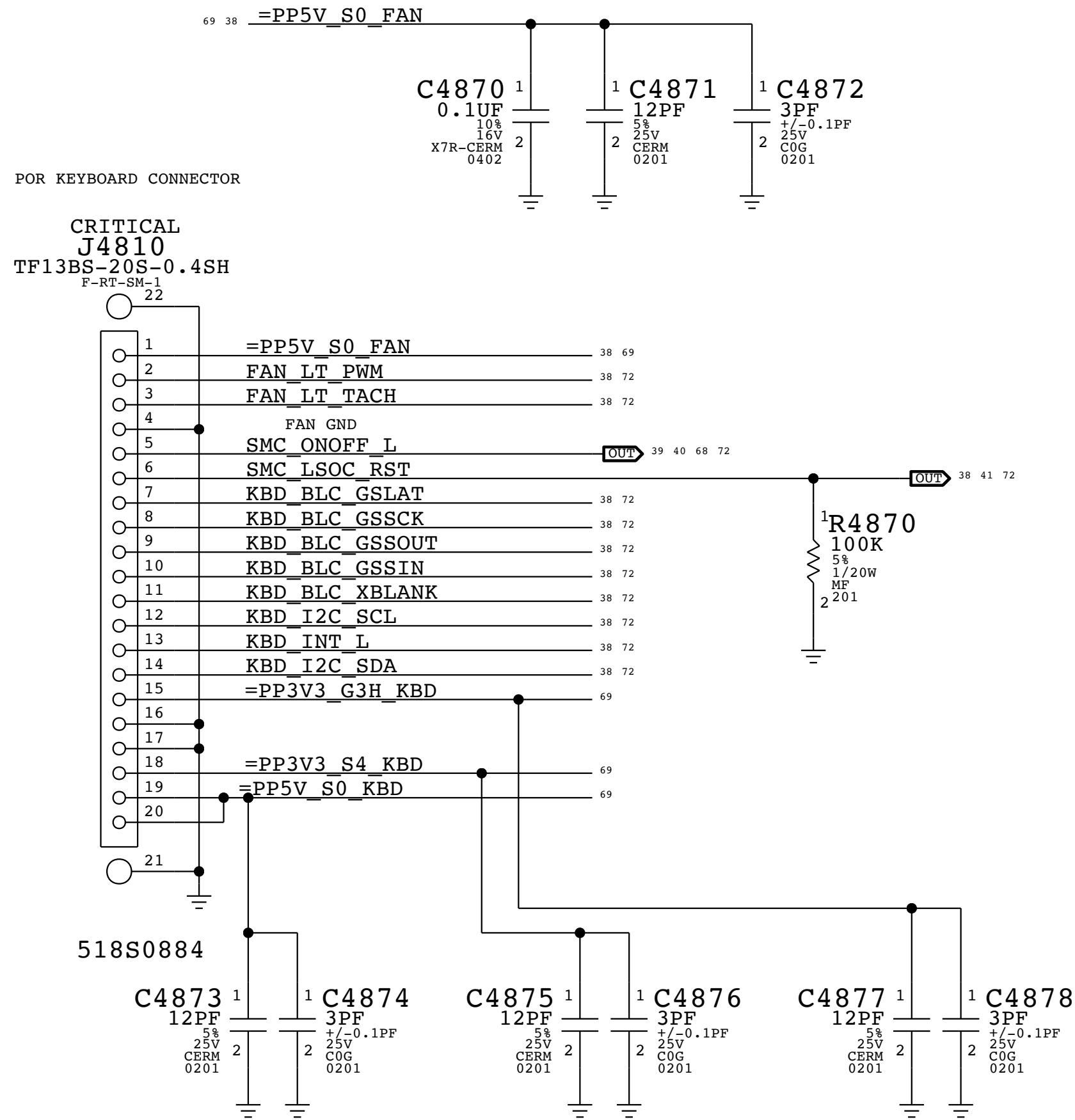
# CAMERA SENSOR



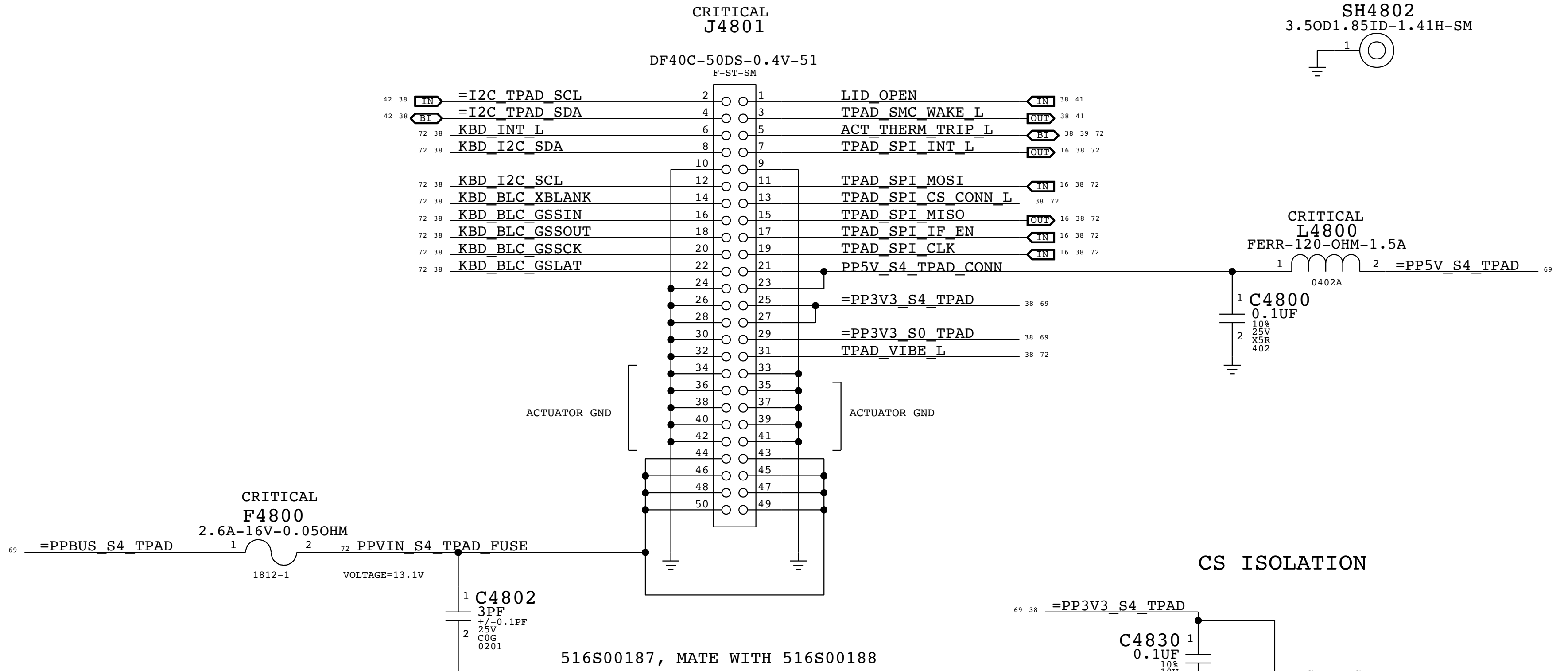
PAGE TITLE			CAMERA 2 OF 2		
		Apple Inc.		DRAWING NUMBER	051-02265
				SIZE	D
				REVISION	1.0.0
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				40 OF 500	
				SHEET	
				37 OF 73	

BOM\_COST\_GROUP=CAMERA

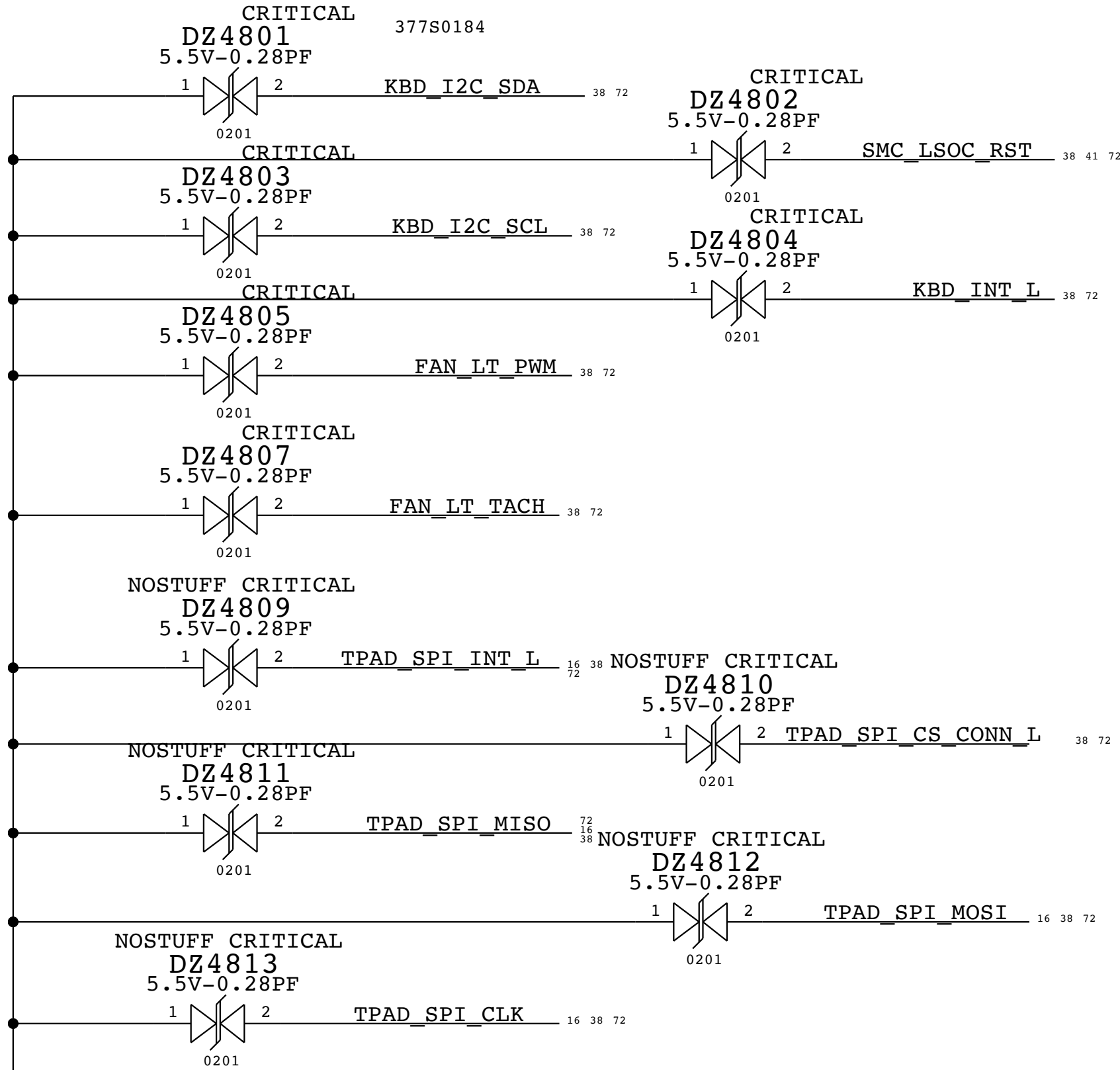
KEYBOARD CONNECTOR



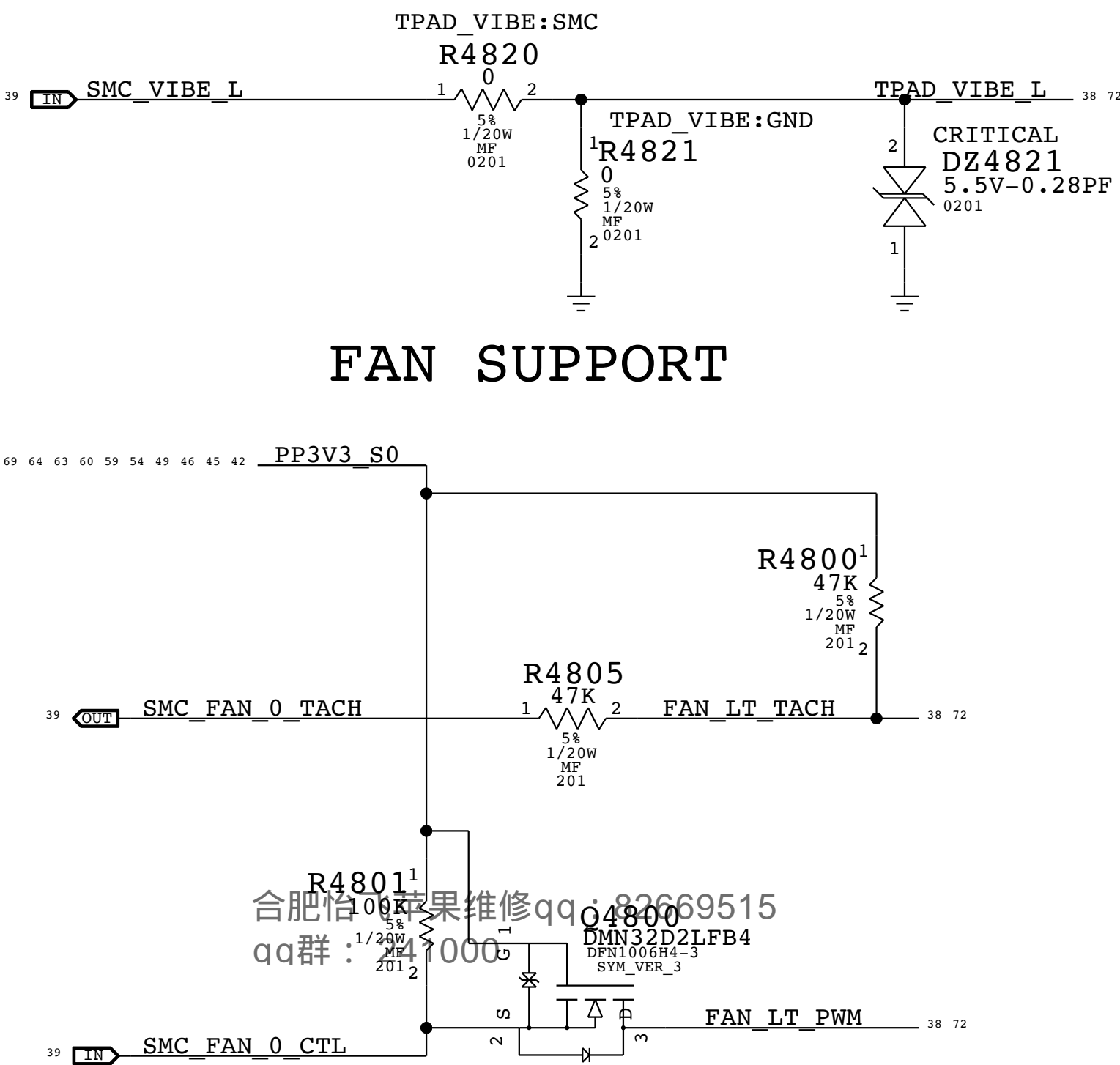
TPAD CONNECTOR




ESD DIODES



FAN SUPPORT



PAGE TITLE		
P1:KEYBOARD & TRACKPAD CONN		
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	REVISION	1.0.0
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BOM\_COST\_GROUP=KEYBOARD



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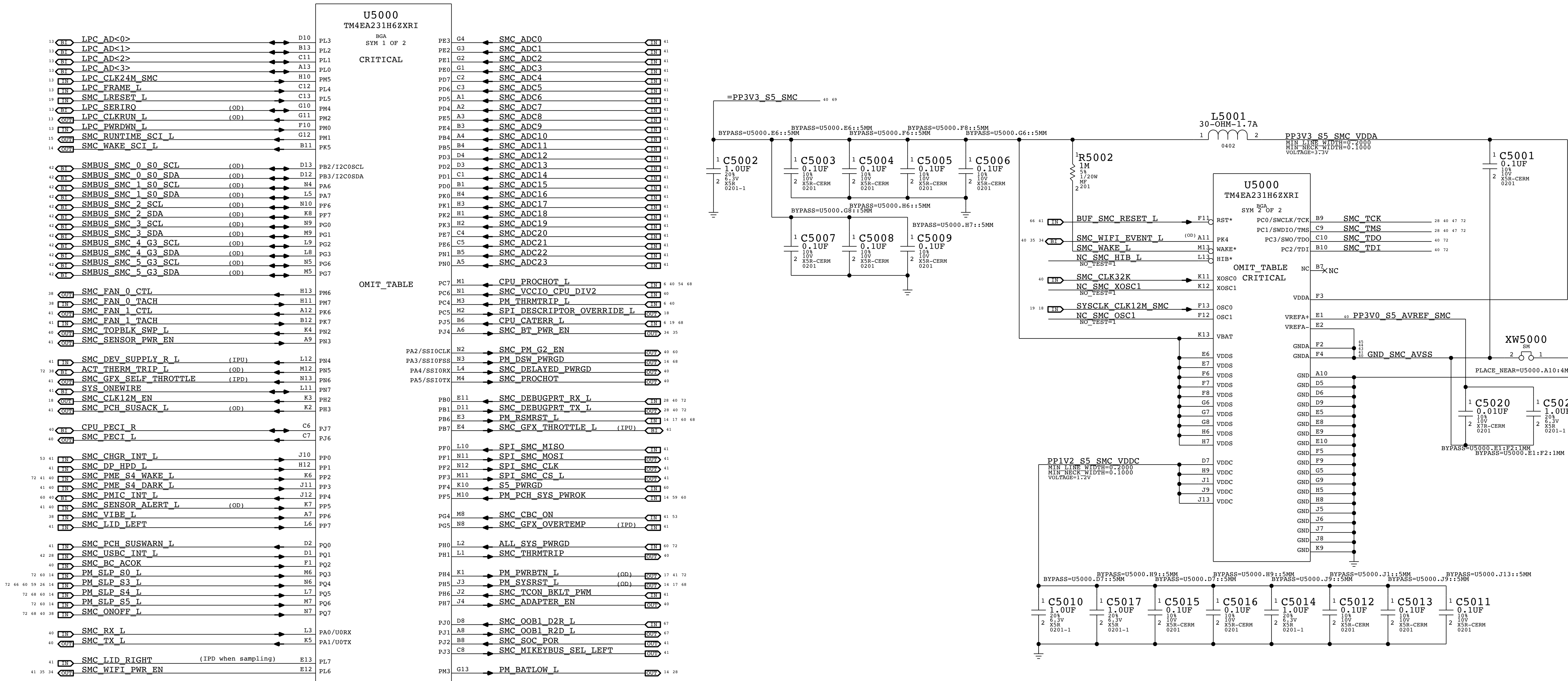
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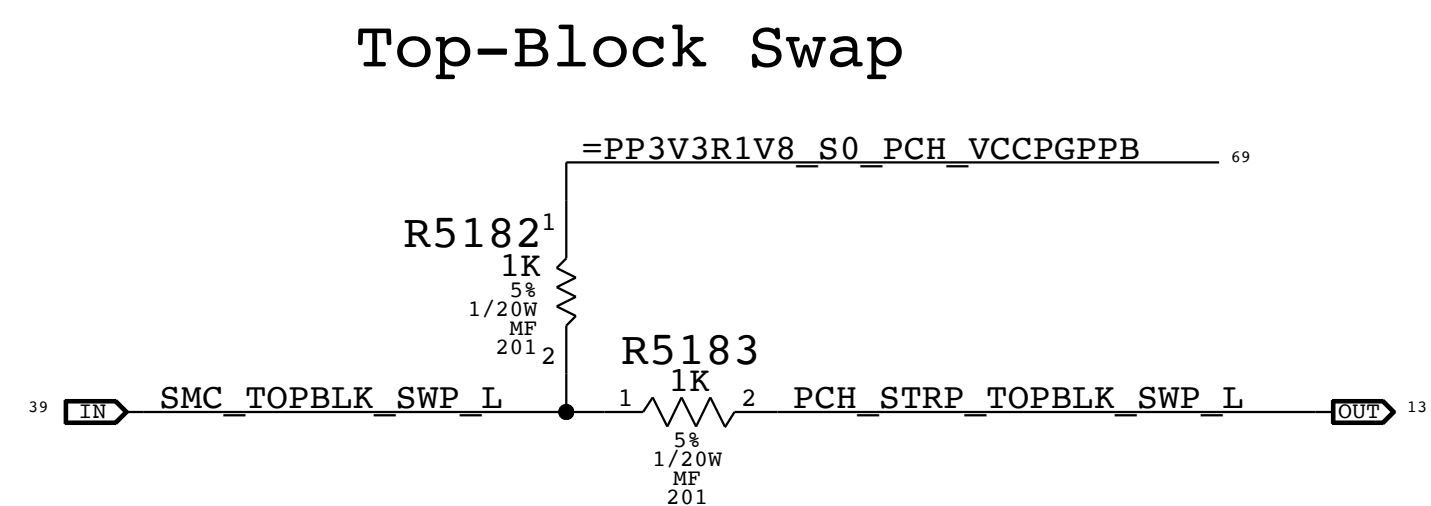
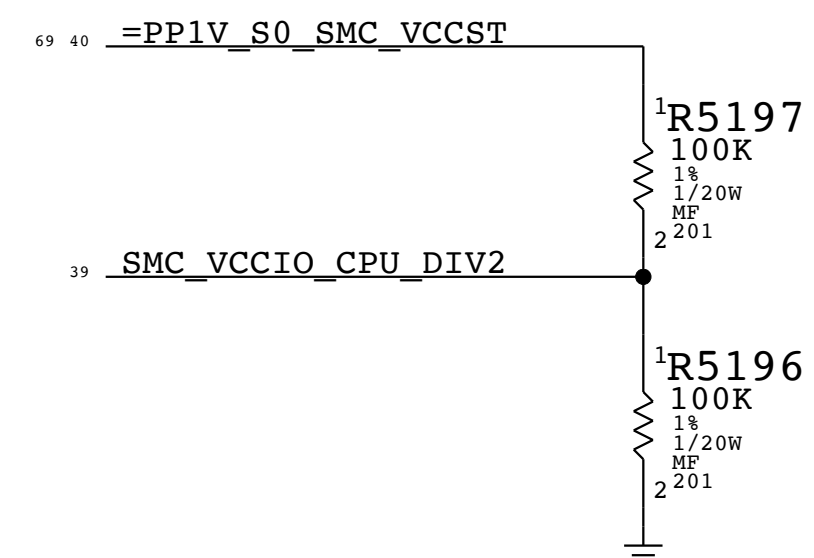
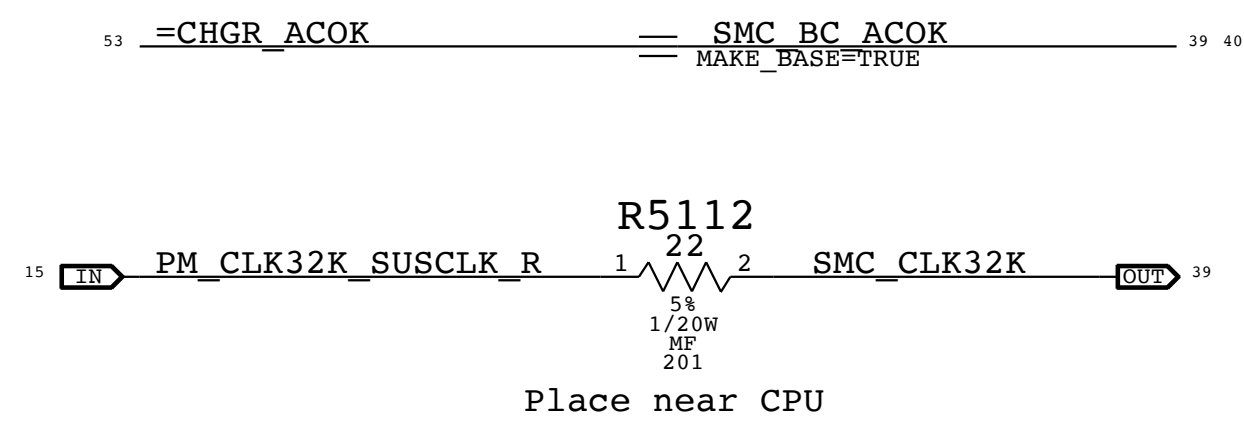
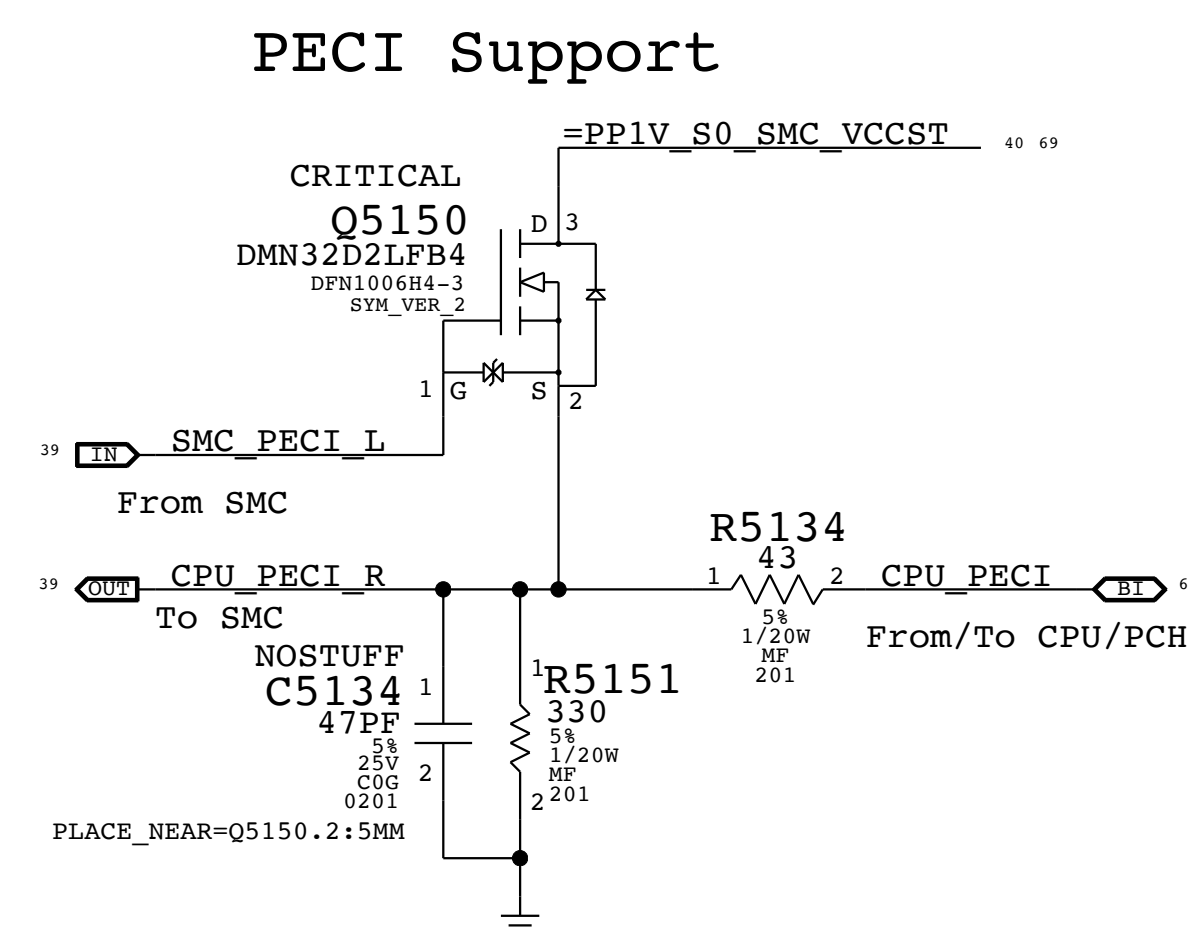
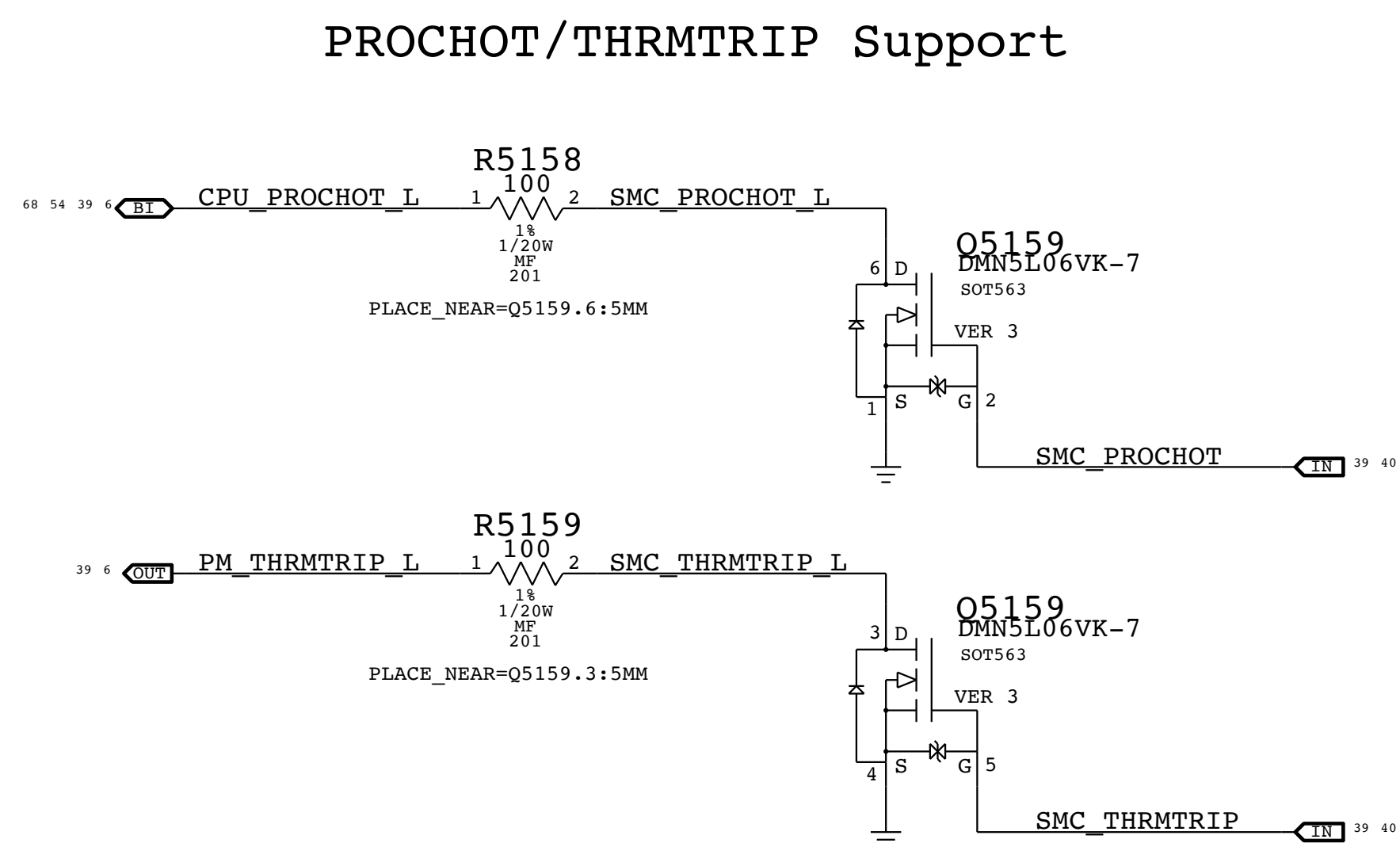
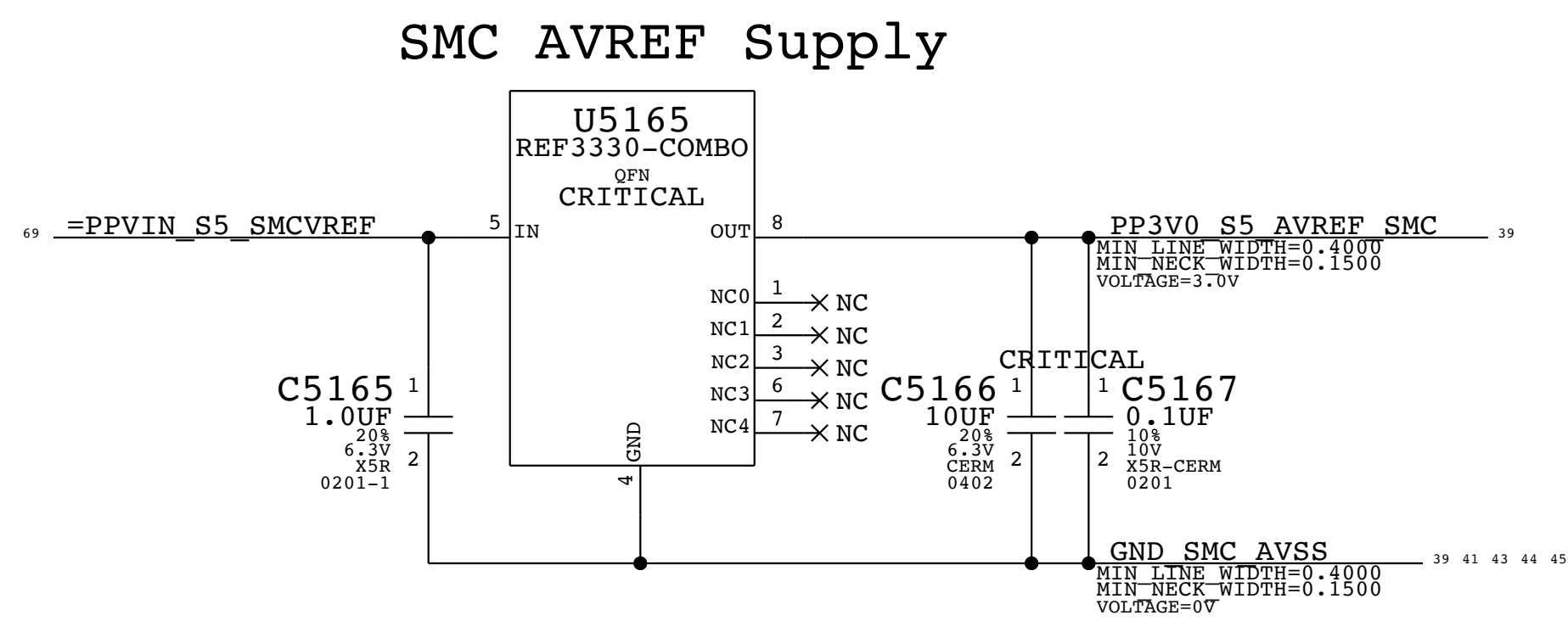
NOTE:  
SMS Interrupt can be active high or low, rename net accordingly.  
If SMS interrupt is not used, pull up to SMC rail.

NOTE:  
Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

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SYNC_MASTER=PAULM		SYNC_DATE=06/15/2015	
PAGE TITLE			
SMC			
 Apple Inc.	DRAWING NUMBER		SIZE
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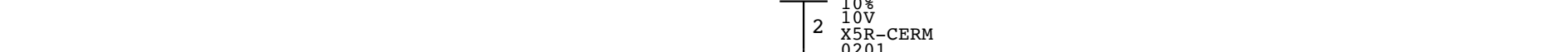
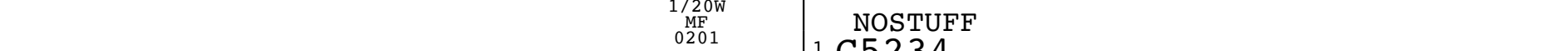
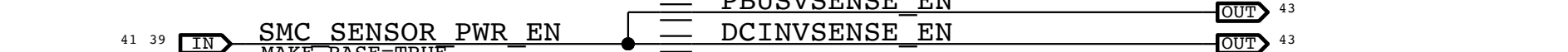
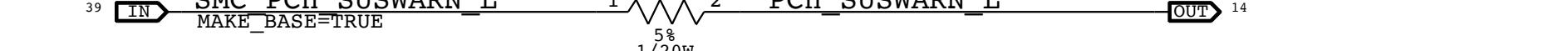
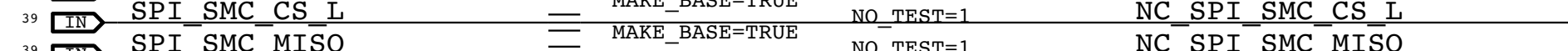
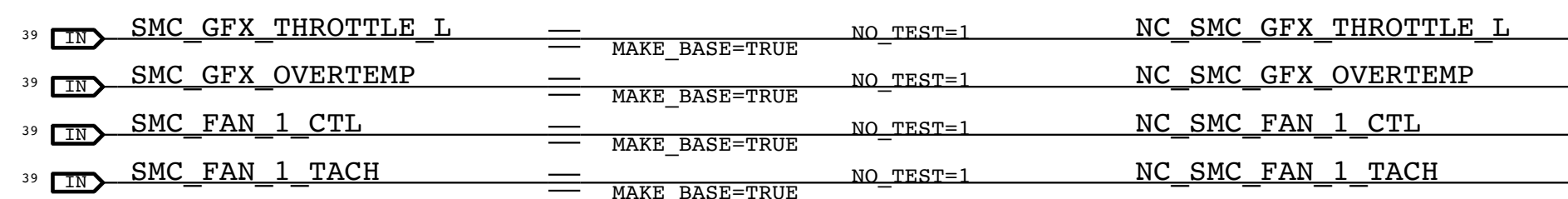
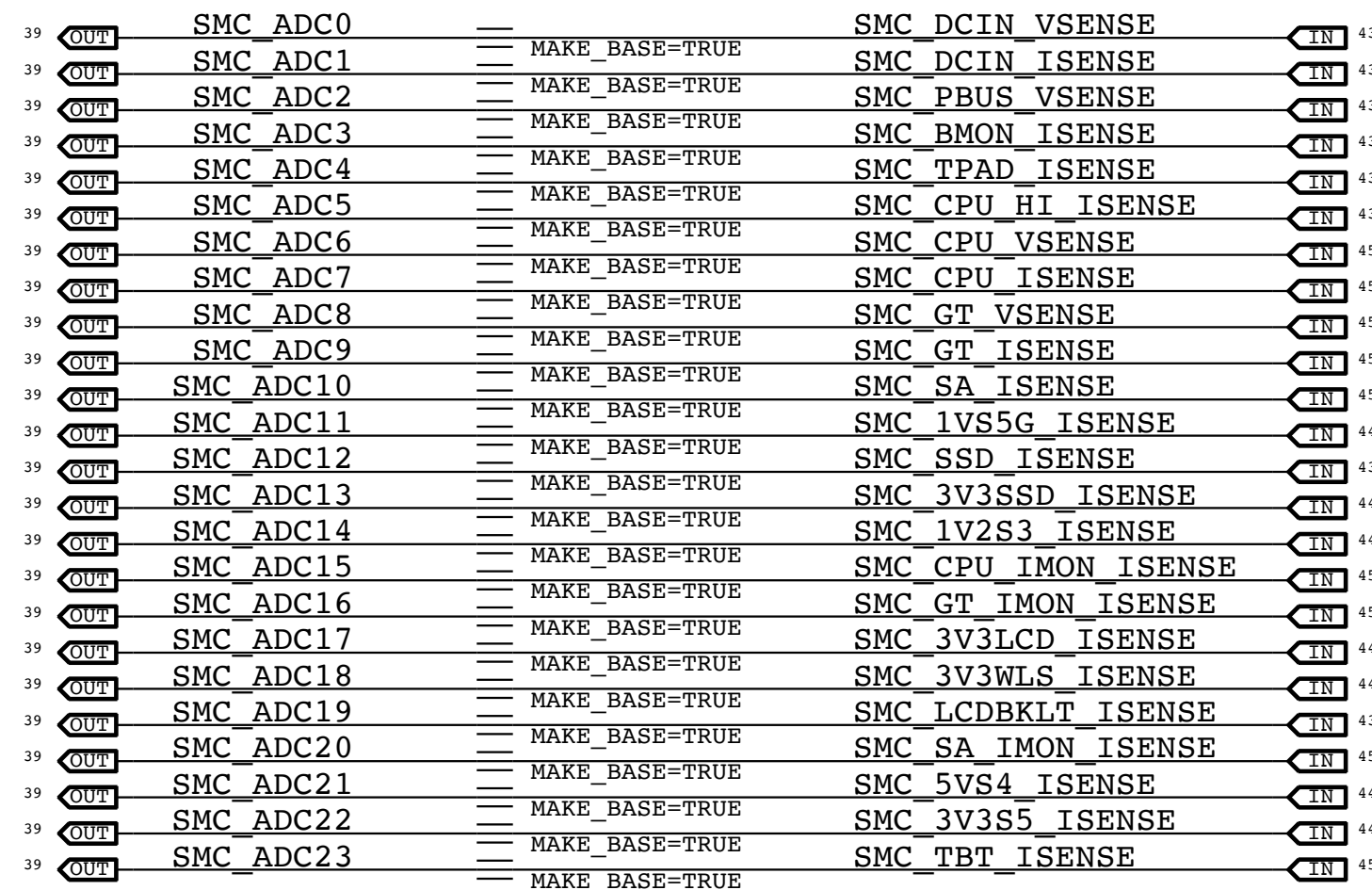


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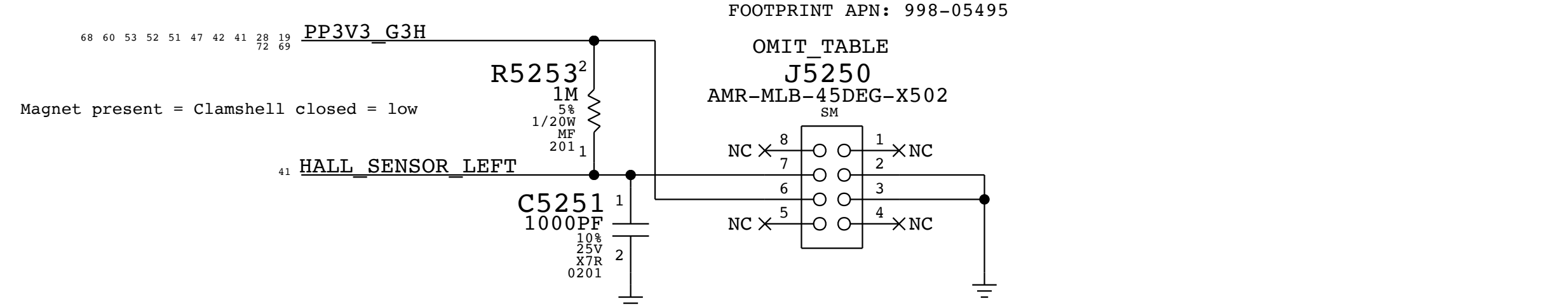
合肥怡飞苹果维修qq : 82669515  
qq群 : 241000

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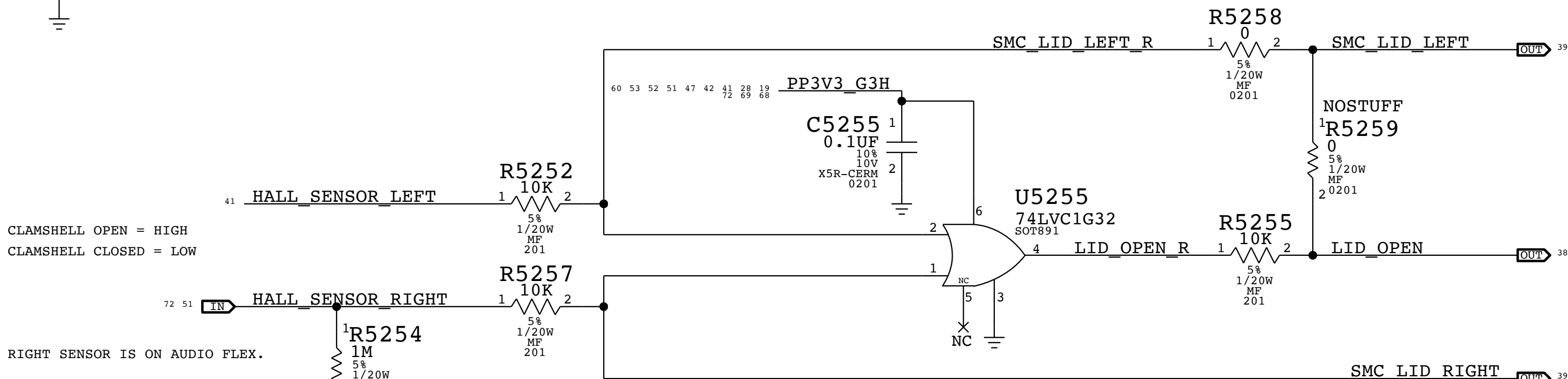
## SMC ANALOG INPUTS



## AMR SENSOR PADS

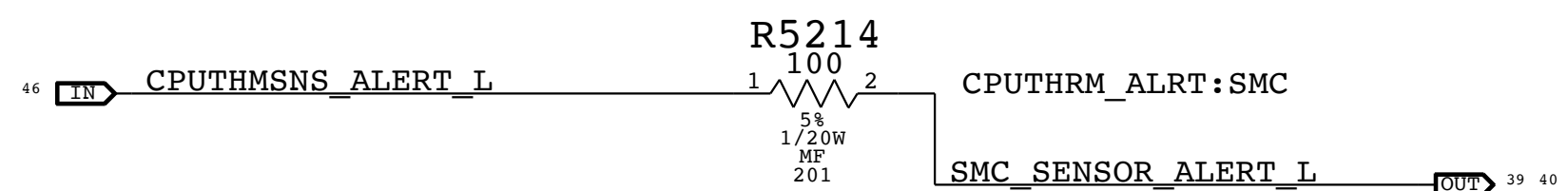


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-05143	1	SUBASSY (T&R) PCBA,HES INTERPOSER 45,X502	J5250	CRITICAL	

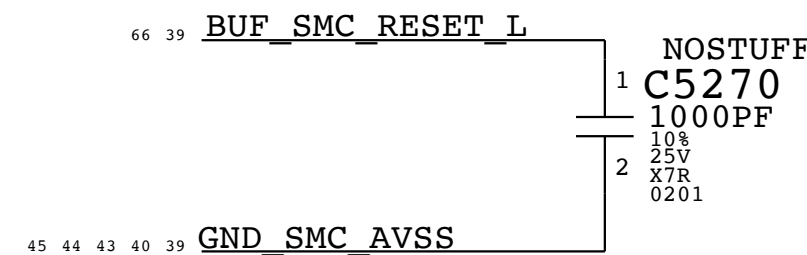
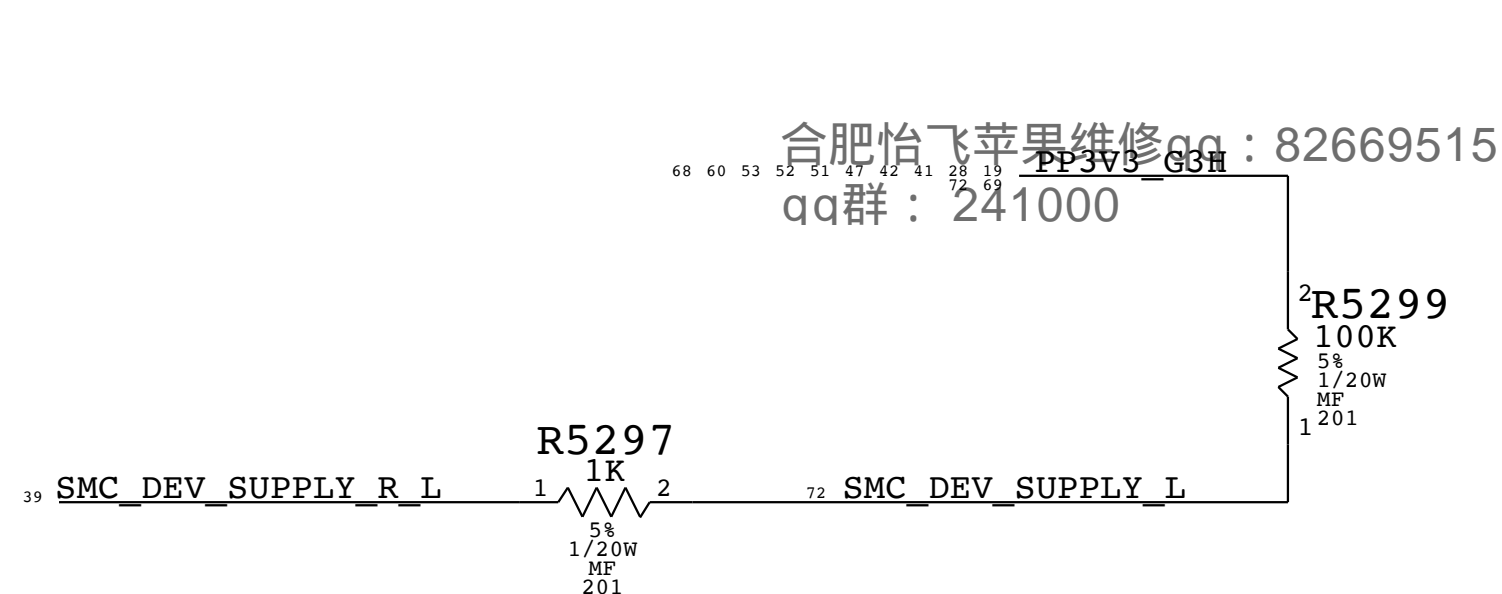
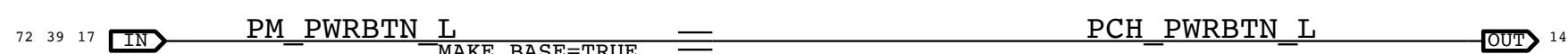
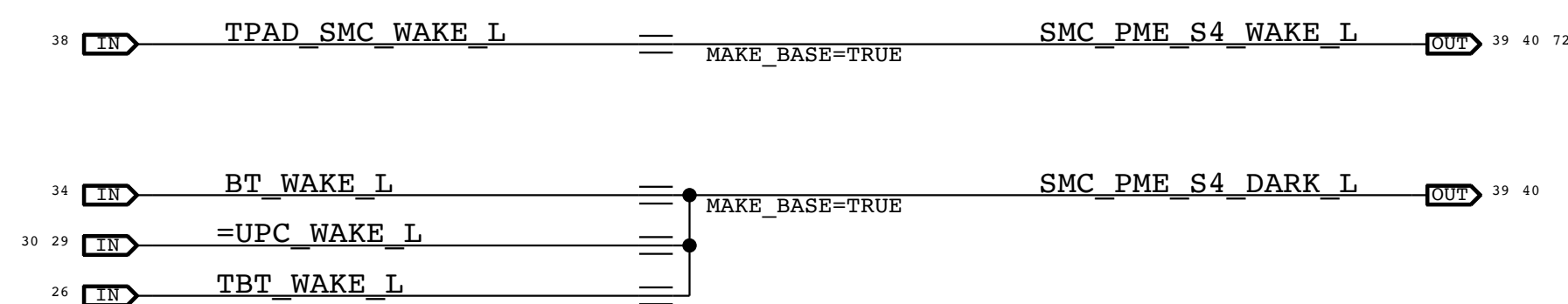


OR gate ensures that both sensors detect that the lid is closed. This prevents a stray magnet from tripping the detect.


## Thermal Alerts



## S4 SMC Wake Sources



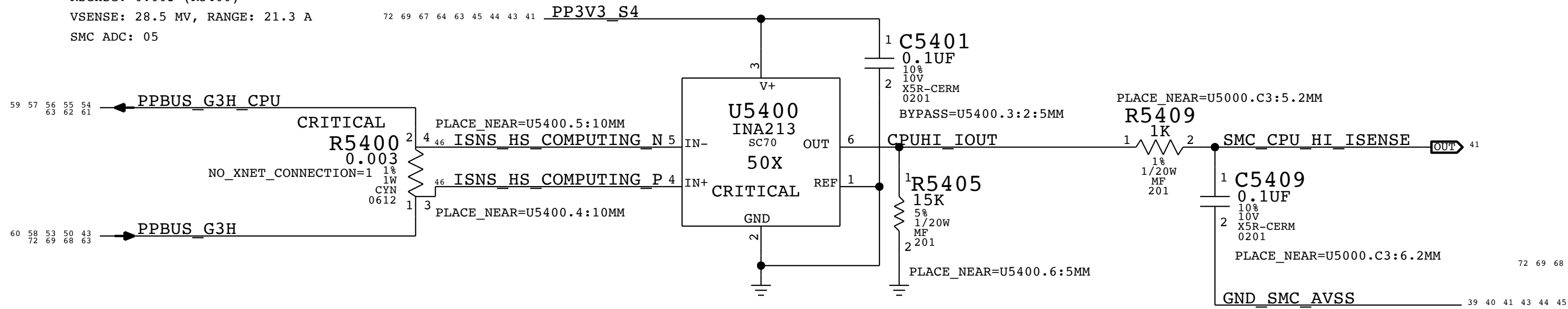
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DESIGN: X502/MLB CATZ		
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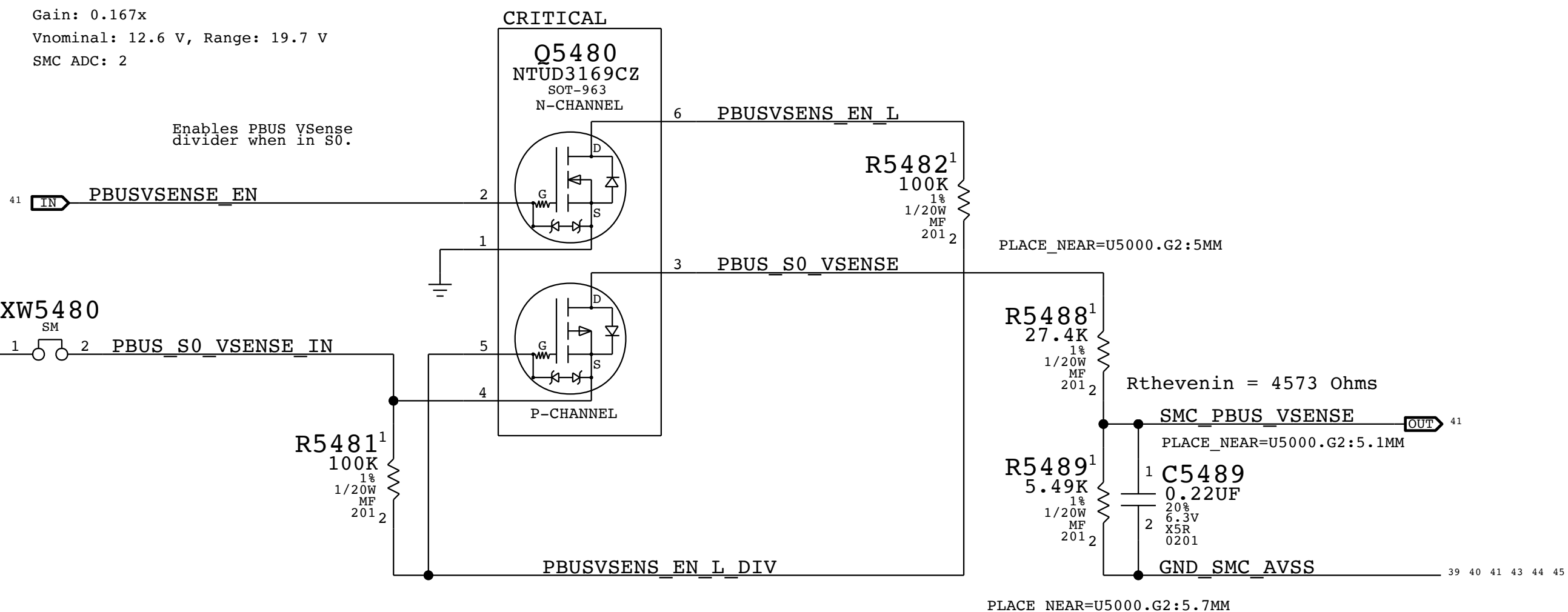
### CPU High Side Current Sense (IC0R)

GAIN: 50X, EDP: 9.5 A  
Rsense: 0.003 (R5400)  
VSENSE: 28.5 MV, RANGE: 21.3 A  
SMC ADC: 05



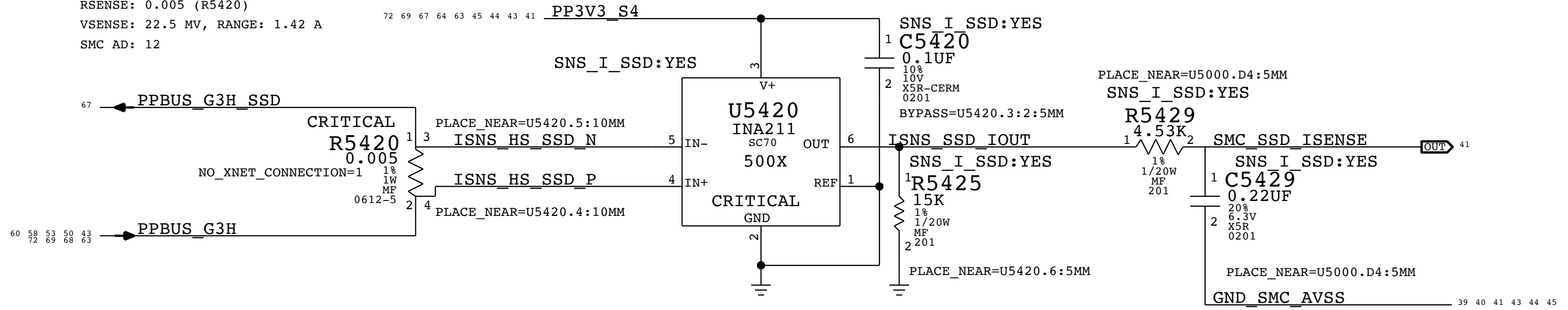
### PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x  
Vnominal: 12.6 V, Range: 19.7 V  
SMC ADC: 2



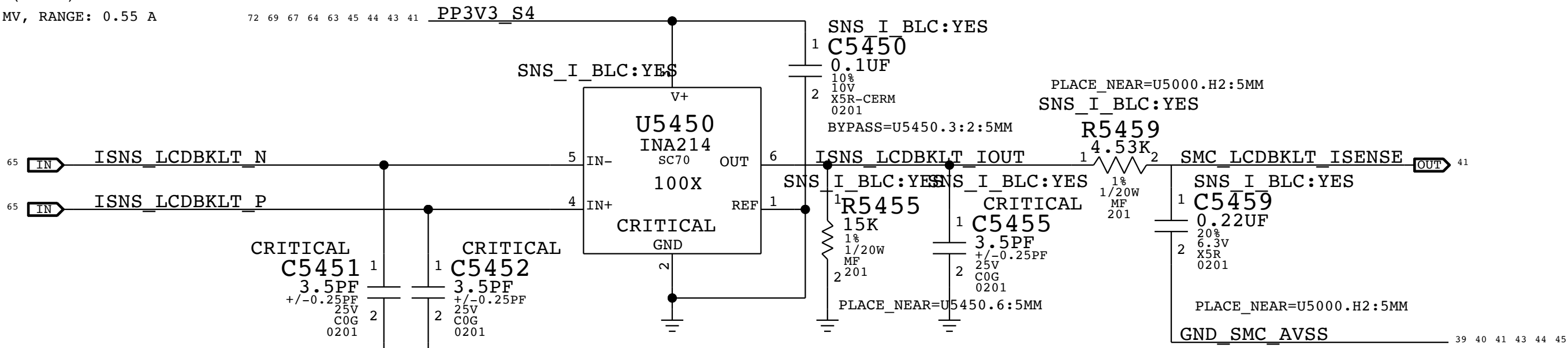
### SSD NAND CURRENT SENSE (IHNC)

GAIN: 500X, EDP: 0.9 A  
RSense: 0.005 (R5420)  
VSENSE: 22.5 MV, RANGE: 1.42 A  
SMC AD: 12



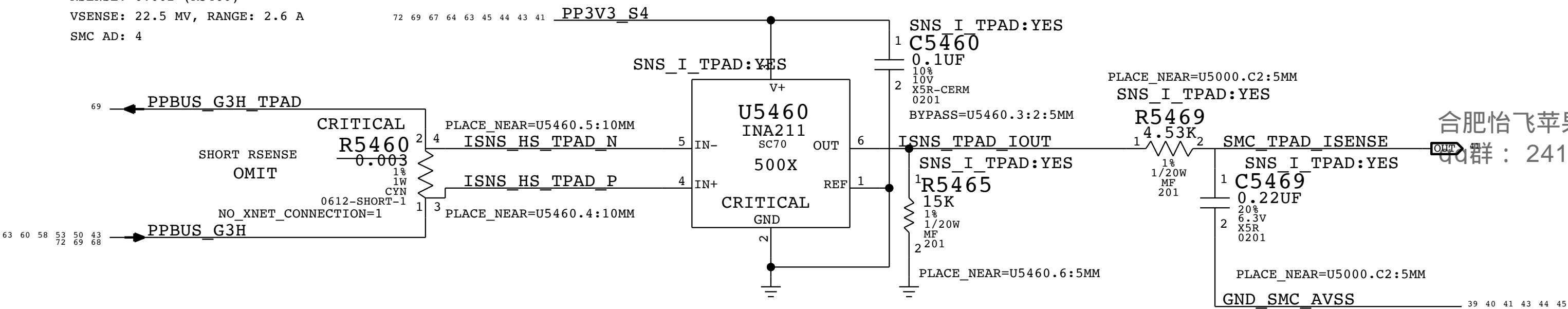
### LCD BACKLIGHT CURRENT SENSE (IBLR)

GAIN: 100X, EDP: 0.9 A  
Rsense: 0.025 (R7700)  
VSENSE: 22.5 MV, RANGE: 0.55 A  
SMC AD: 19



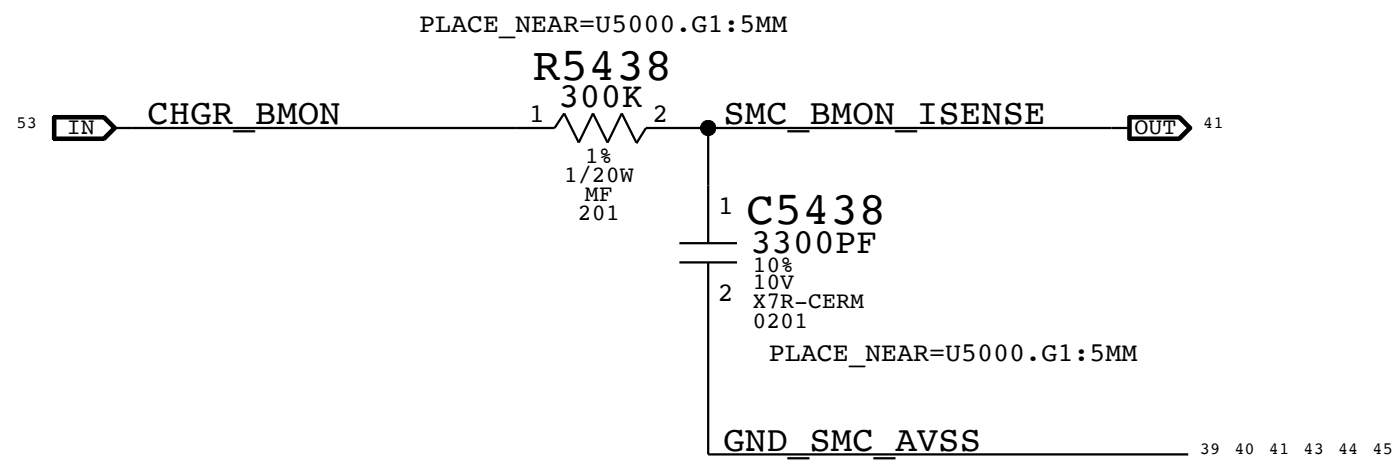
### TRACKPAD ACTUATOR X239 CURRENT SENSE (ITAR)

GAIN: 200X, EDP: 0.9 A  
RSense: 0.002 (R5460)  
VSENSE: 22.5 MV, RANGE: 2.6 A  
SMC AD: 4



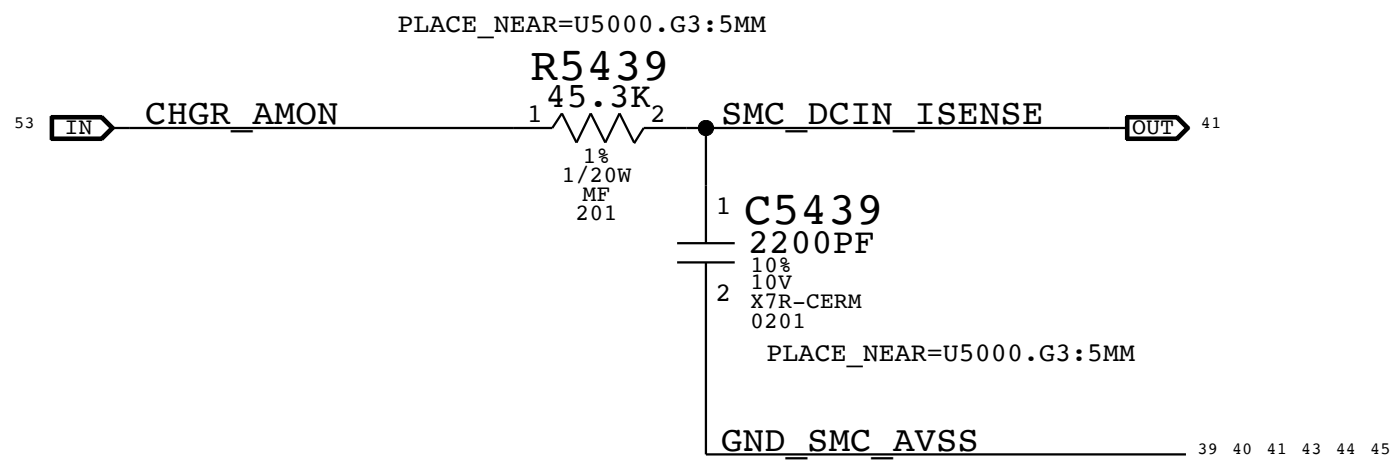
### Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A  
RSense: 0.005 (R7160)  
SMC ADC: 03



### DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A  
RSense: 0.010 (R7120)  
SMC ADC: 01



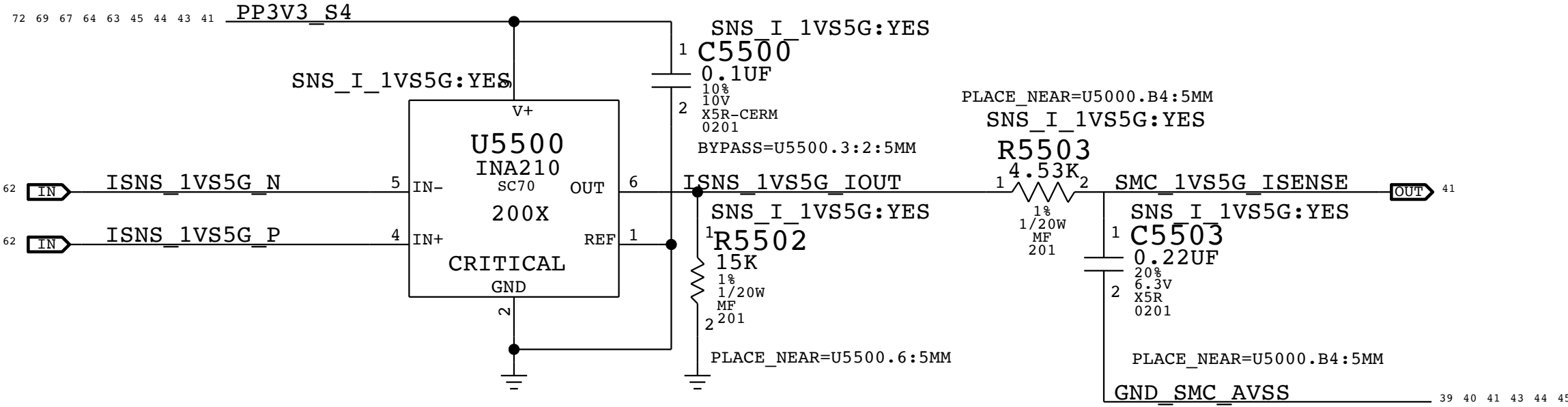
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117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		SNS_I_BLC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		SNS_I_TPAD:NO

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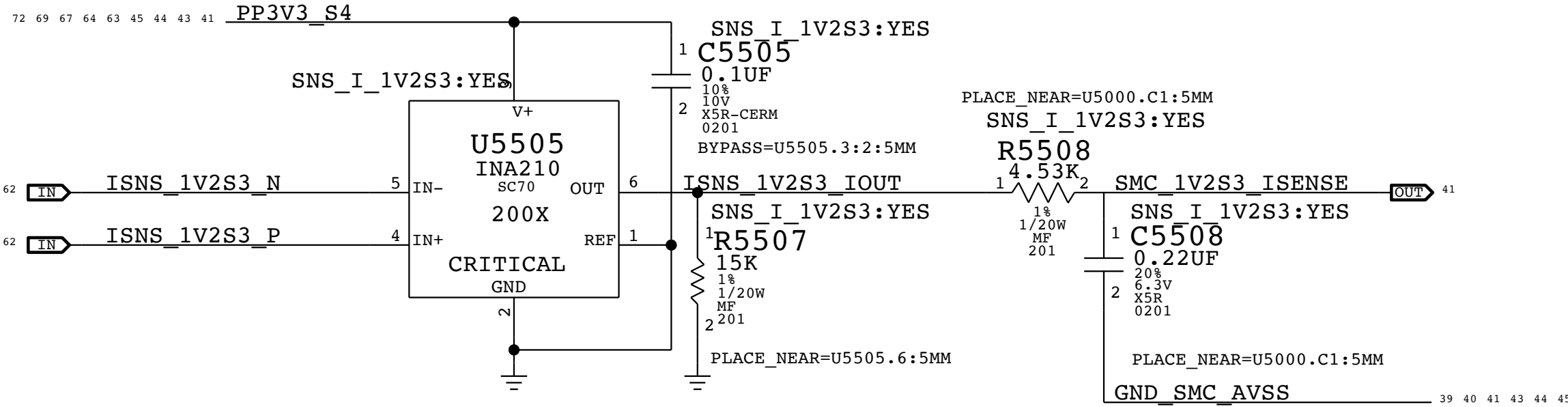
1V\_S5G CURRENT SENSE (ISIC)

GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.003 (R7700)  
VSENSE: 22.5 MV, RANGE: 3.0 A  
SMC AD: 11



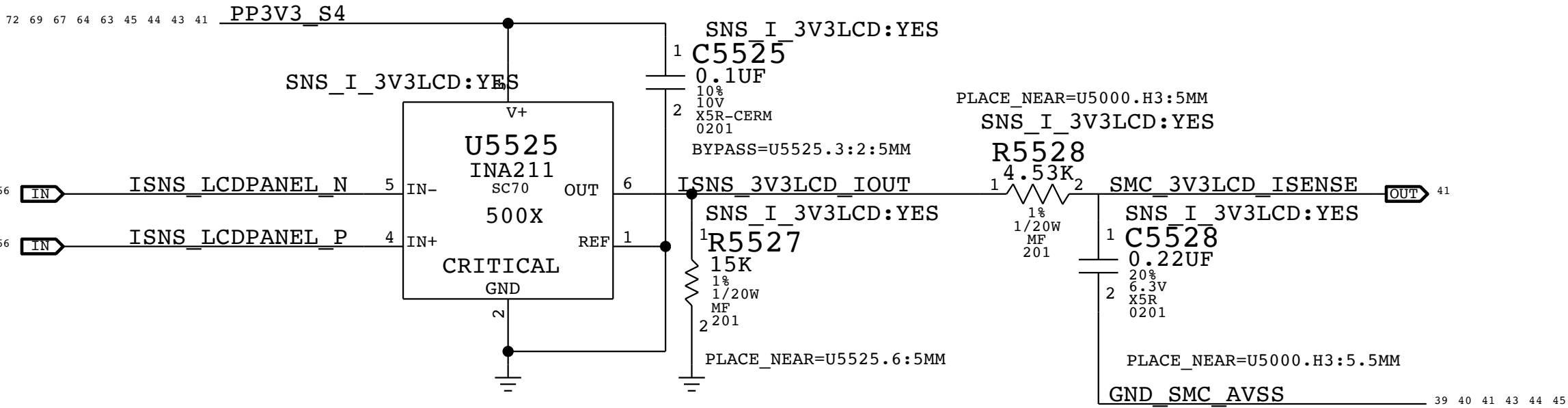
1V2\_S3 CURRENT SENSE (IMOC)

GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.002 (R7700)  
VSENSE: 22.5 MV, RANGE: 7.67 A  
SMC AD: 14



3V3\_S0 LCD CURRENT SENSE (ILDC)

GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.005 (R5525)  
VSENSE: 22.5 MV, RANGE: 1.6 A  
SMC AD: 17

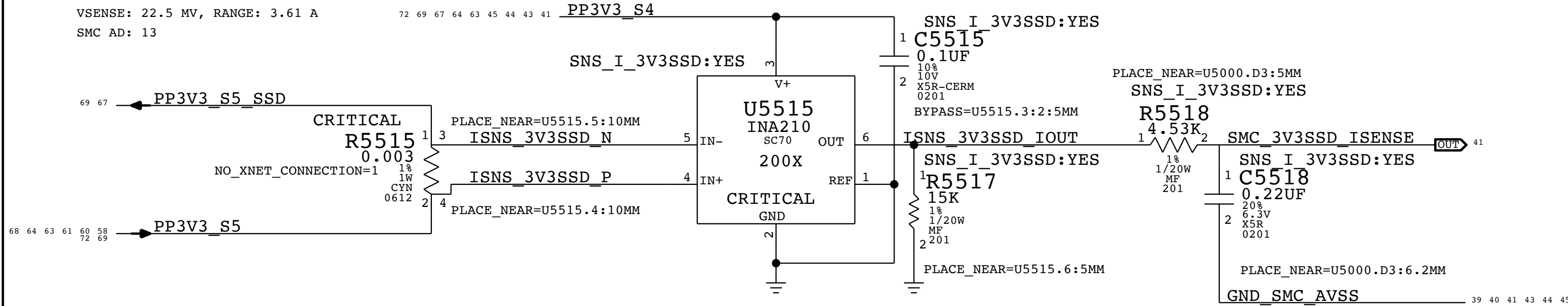


5V\_S0 LCD CURRENT SENSE (I\_\_\_)

GAIN: 500X. EDP: 0.9 A  
RSENSE: 0.005 (R8520)  
VSENSE: 22.5 MV, RANGE: 1.6 A  
SMC AD: 17

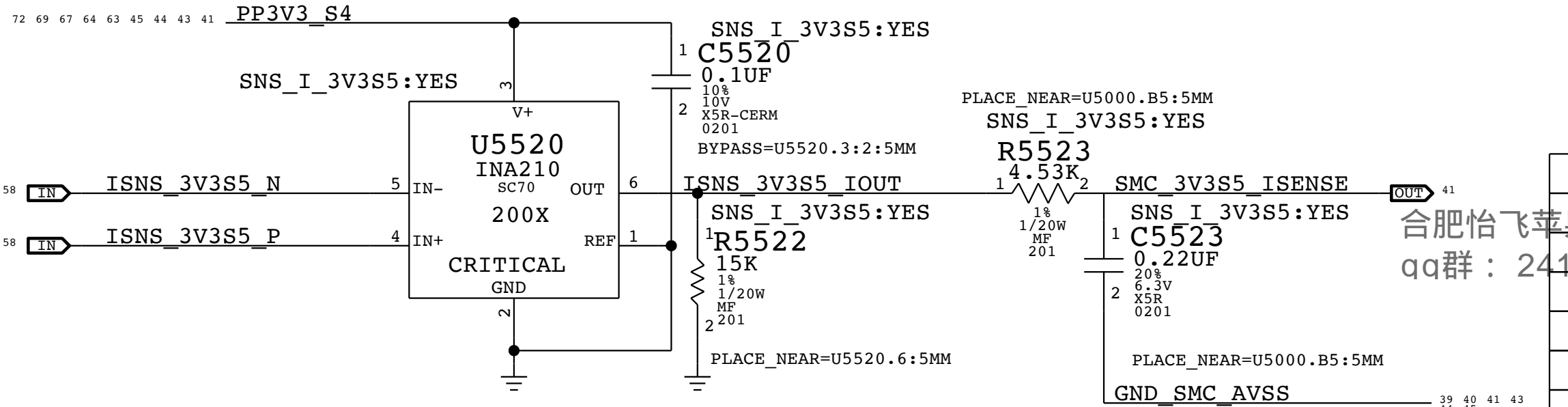
3V3\_SSD CURRENT SENSE (IHCC)

GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.003 (R5515)  
VSENSE: 22.5 MV, RANGE: 3.61 A  
SMC AD: 13



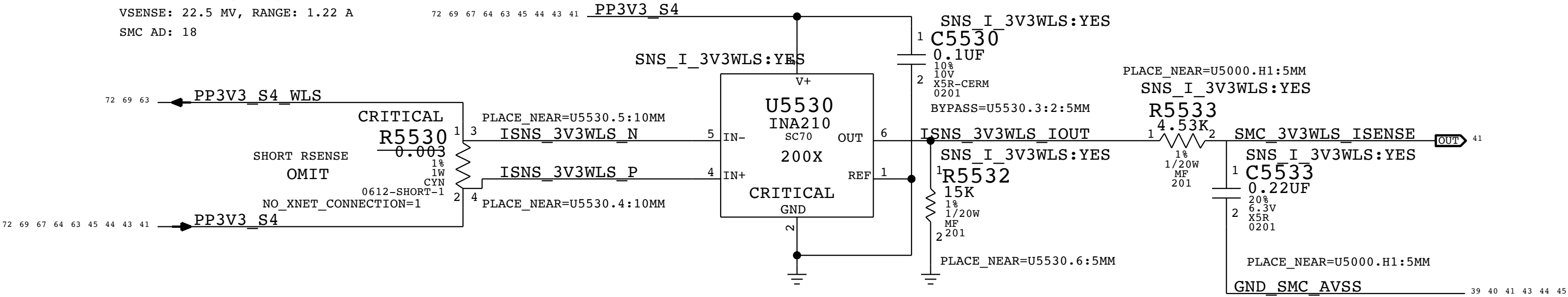
3V3\_S5 CURRENT SENSE (IO3R)

GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.003 (R7710)  
VSENSE: 22.5 MV ?, RANGE: 4 A  
SMC AD: 22



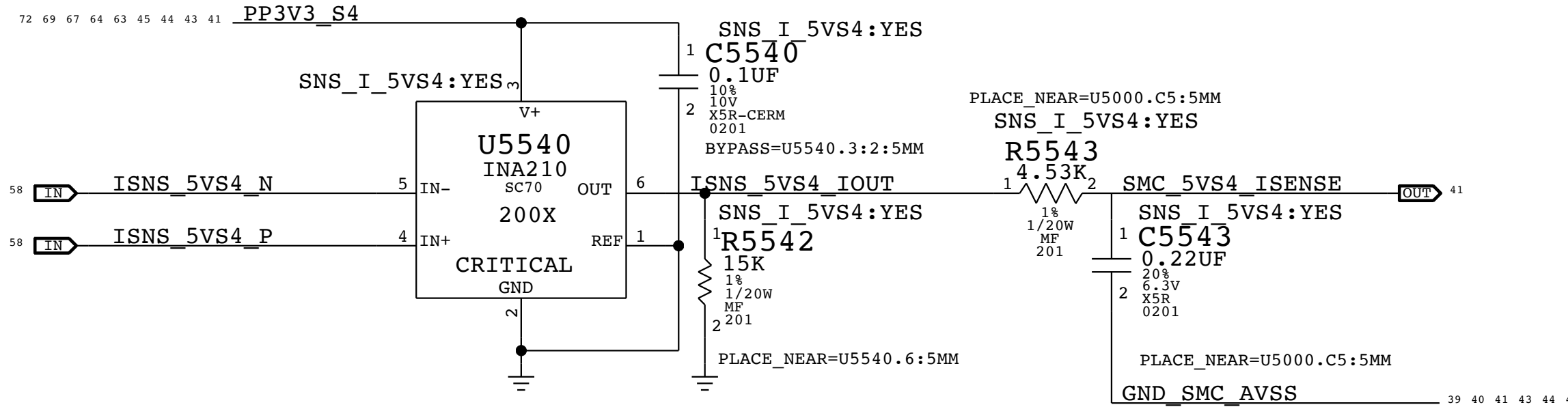
3V3\_S4 WIRELESS CURRENT SENSE (IAPC)

GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.010 (R7700)  
VSENSE: 22.5 MV, RANGE: 1.22 A  
SMC AD: 18



5V\_S4 CURRENT SENSE (IO5R)

GAIN: 200X. EDP: ?? A  
RSENSE: 0.003 (R7900)  
VSENSE: 22.5 MV ?, RANGE: 6.8 A  
SMC AD: 21



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5508		SNS_I_1V2S3:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5518		SNS_I_3V3SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5523		SNS_I_3V3S5:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5528		SNS_I_3V3LCD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5533		SNS_I_3V3WLS:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5543		SNS_I_5VS4:NO

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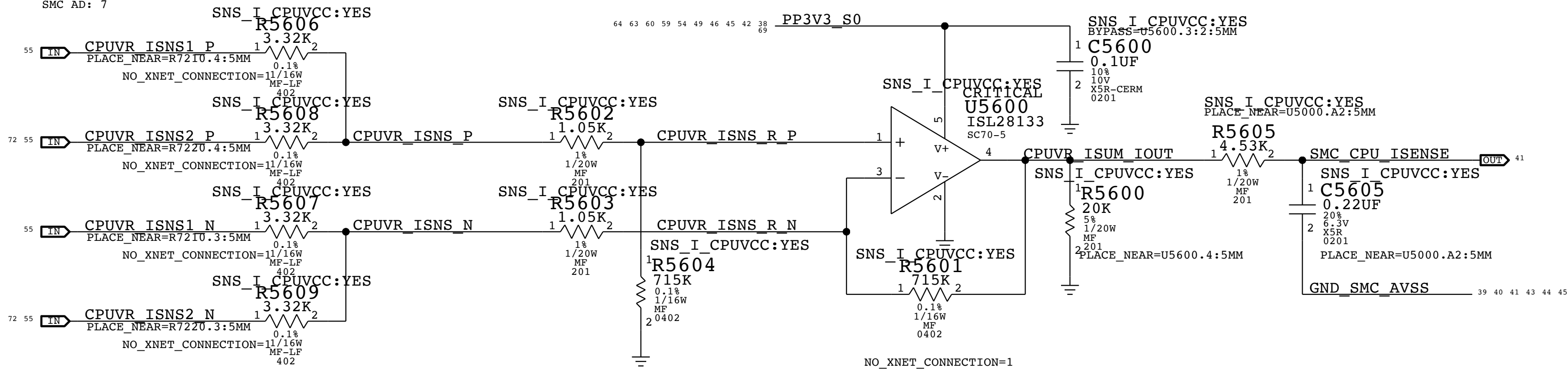
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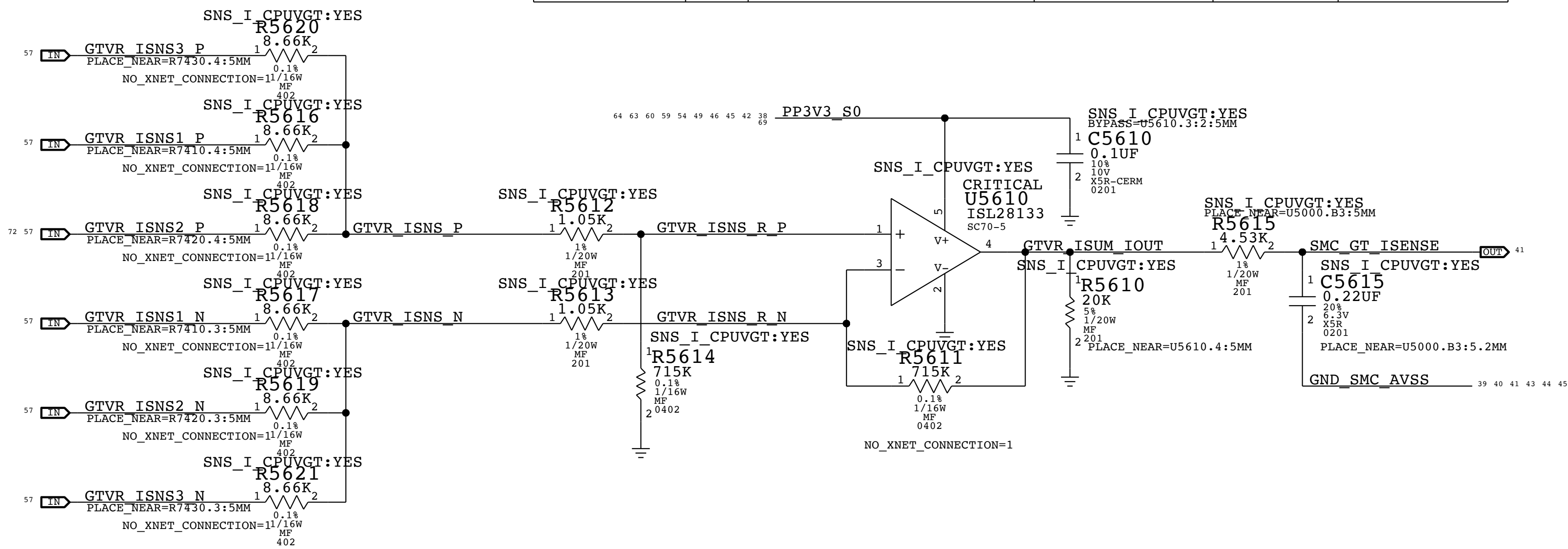
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GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.005 (R7700)  
VSENSE: 22.5 MV, RANGE: 2.27 A  
SMC AD: 7



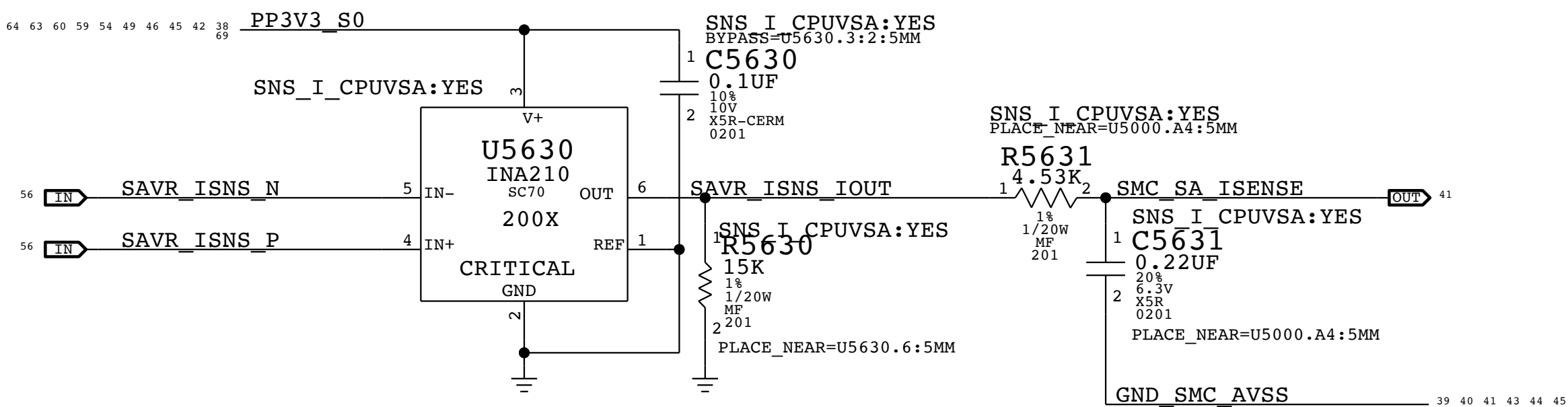
## CPU GT CURRENT SENSE (ICGC)

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RSENSE: 0.005 (R7700)  
VSENSE: 22.5 MV, RANGE: 2.27 A  
SMC AD: 9



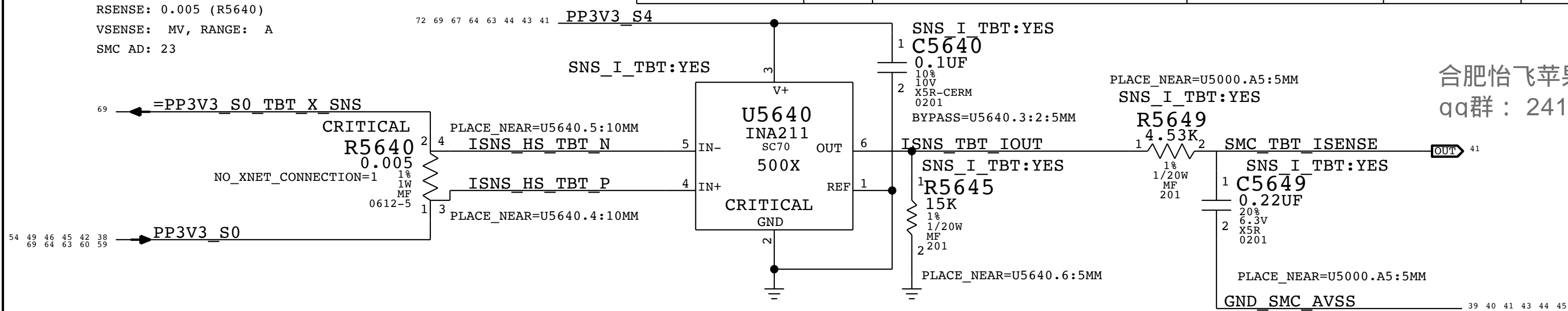
## CPU SA CURRENT SENSE (ICSC)

GAIN: 200X. EDP: 0.9 A  
RSENSE: 0.002 (R7700)  
VSENSE: 22.5 MV, RANGE: 7.67 A  
SMC AD: 10



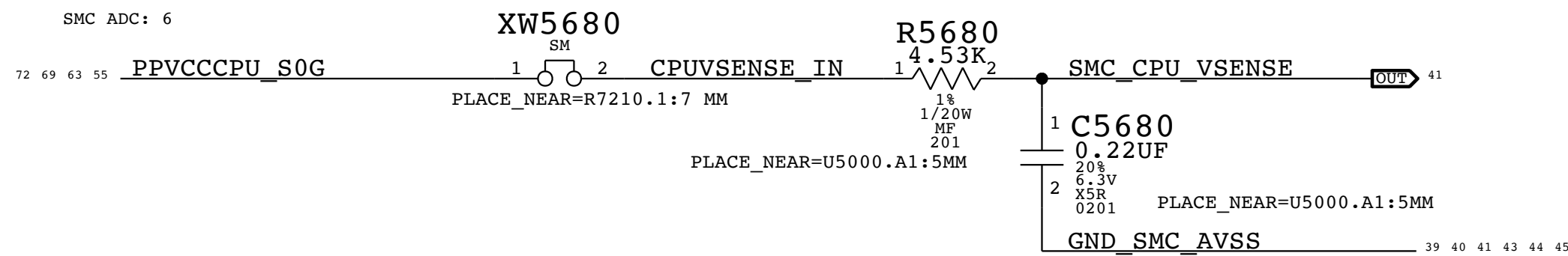
## TBT CURRENT SENSE (IULC)

GAIN: 500X. EDP: A  
RSENSE: 0.005 (R5640)  
VSENSE: MV, RANGE: A  
SMC AD: 23



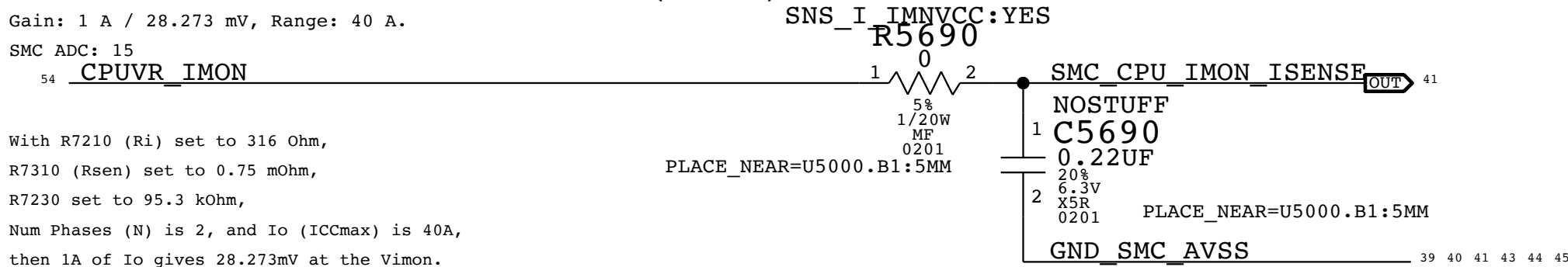
## CPU CORE VOLTAGE SENSE (VCAC)

SMC ADC: 6



## CPU CORE IMON CURRENT SENSE (ICAM)

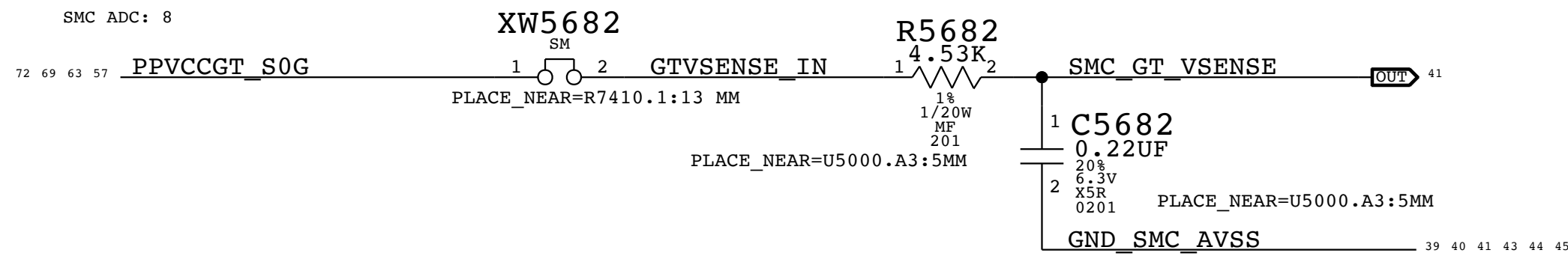
Gain: 1 A / 28.273 mV, Range: 40 A.  
SMC ADC: 15



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5605		SNS_I_CPUVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5615		SNS_I_CPUVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5631		SNS_I_CPUVSA:NO

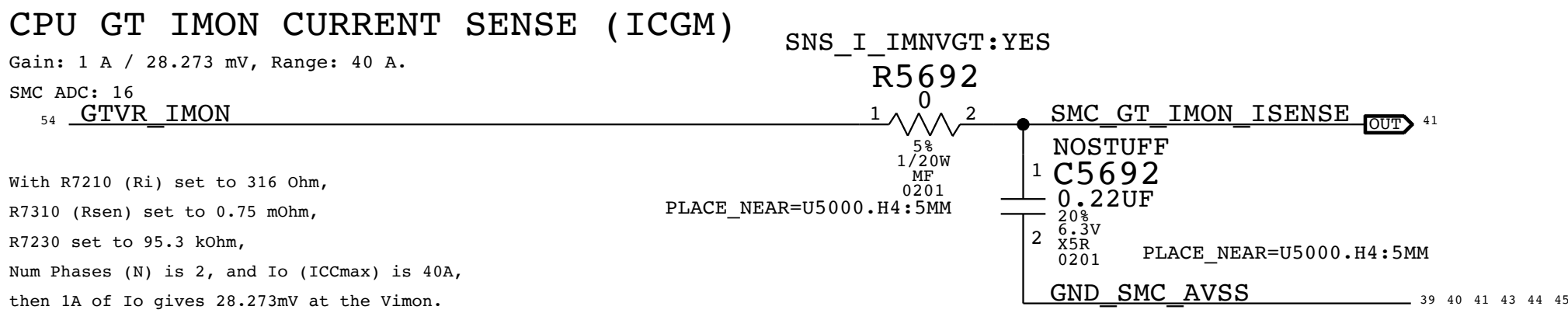
## CPU GT VOLTAGE SENSE (VCGC)

SMC ADC: 8



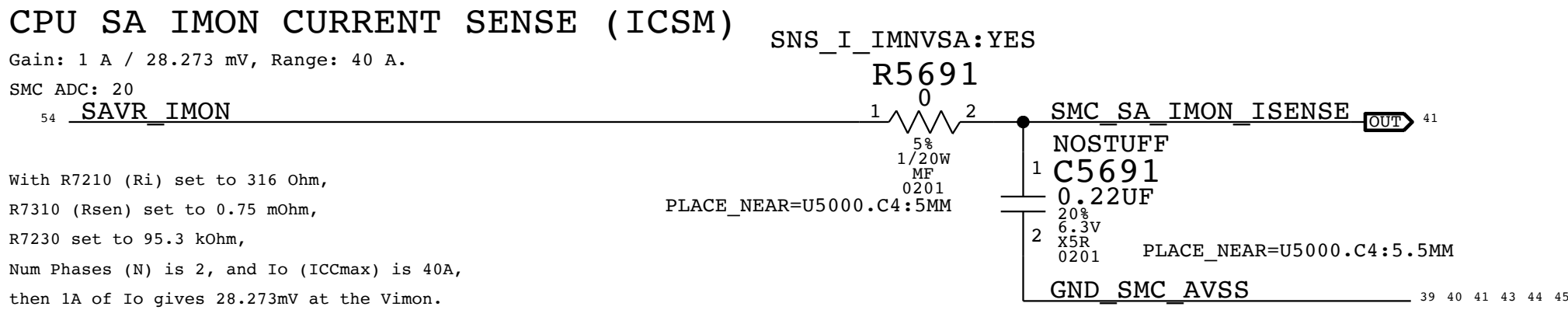
## CPU GT IMON CURRENT SENSE (ICGM)

Gain: 1 A / 28.273 mV, Range: 40 A.  
SMC ADC: 16



## CPU SA IMON CURRENT SENSE (ICSM)

Gain: 1 A / 28.273 mV, Range: 40 A.  
SMC ADC: 20



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5649		SNS_I_TBT:NO

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qq群 : 241000

DESIGN: X502/MLB CATZ		
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Power Sensors Extended		
	DRAWING NUMBER	051-02265
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BOM\_COST\_GROUP=SENSORS

8

7

6

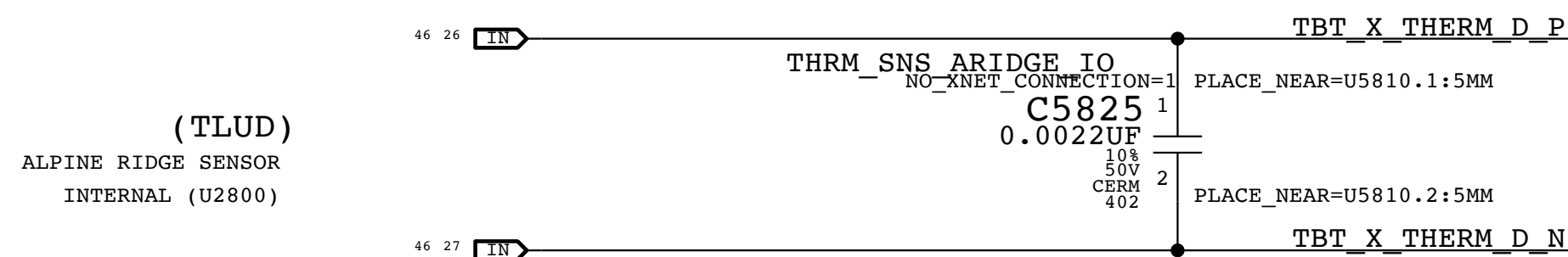
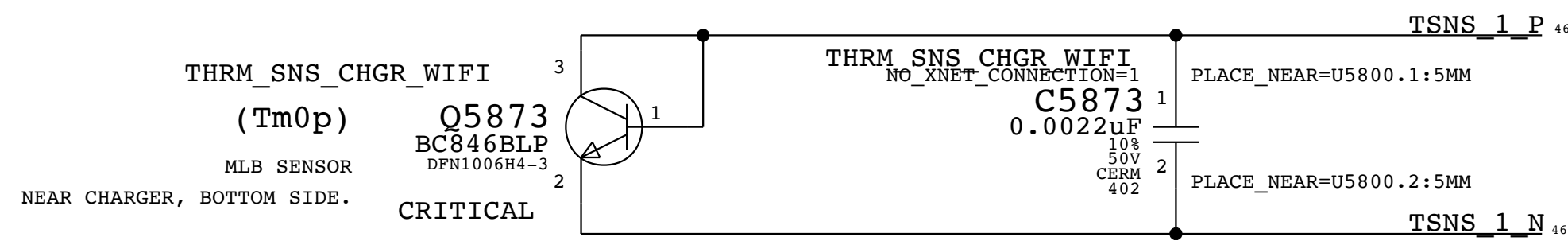
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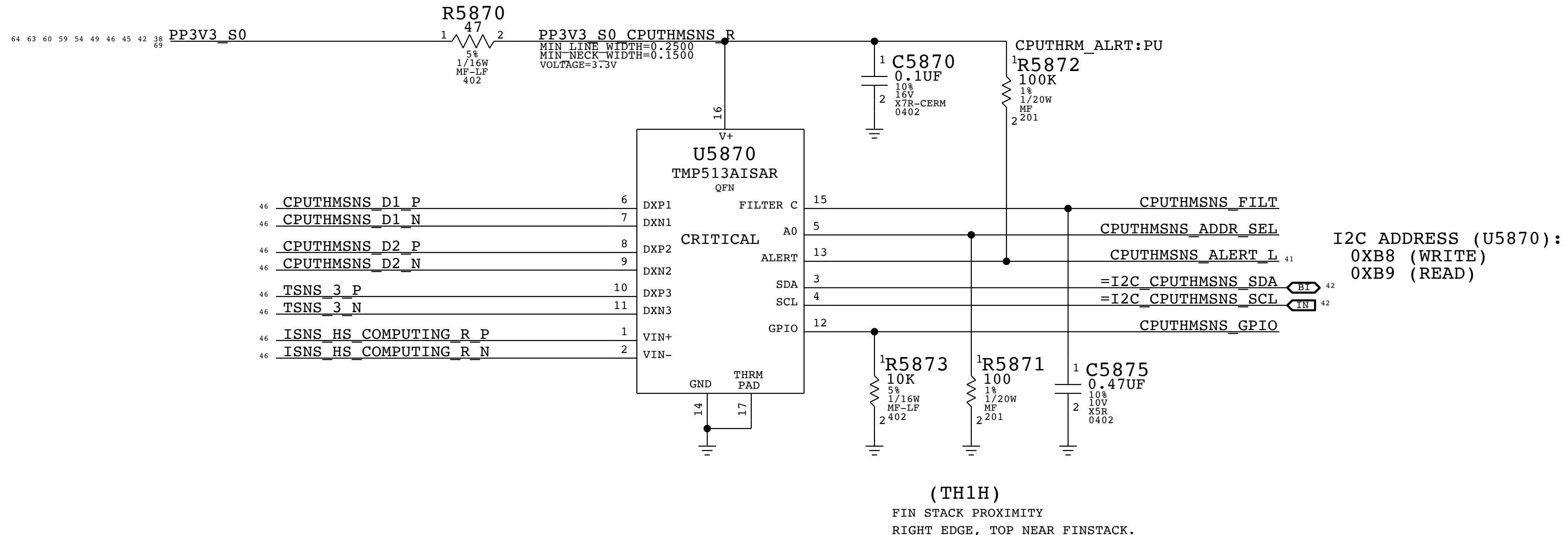
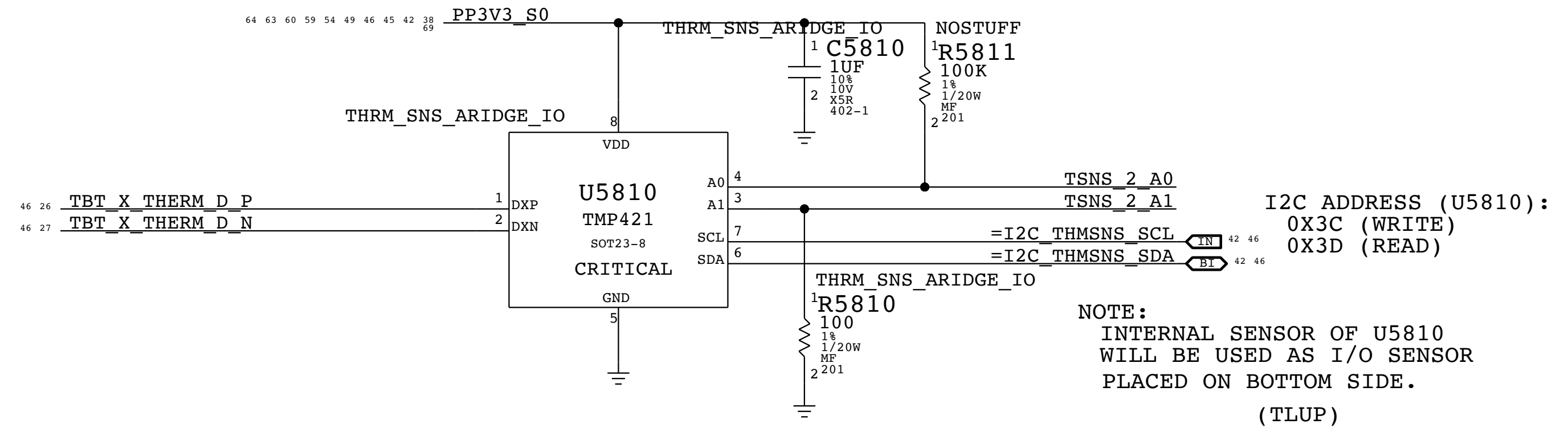
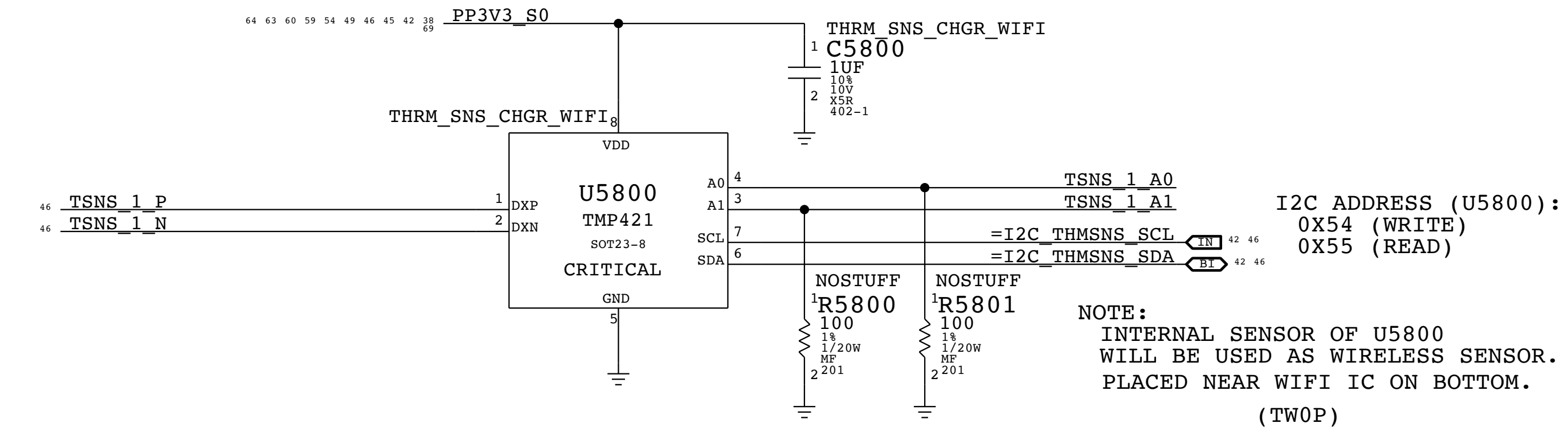
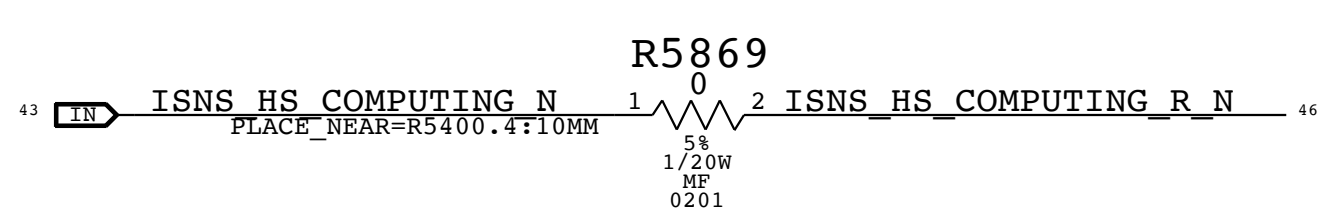
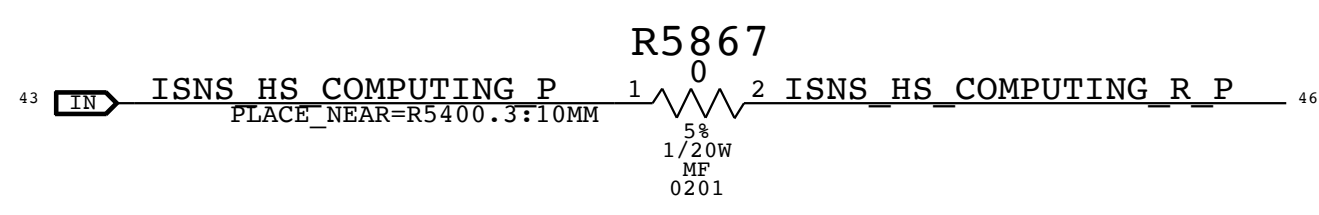
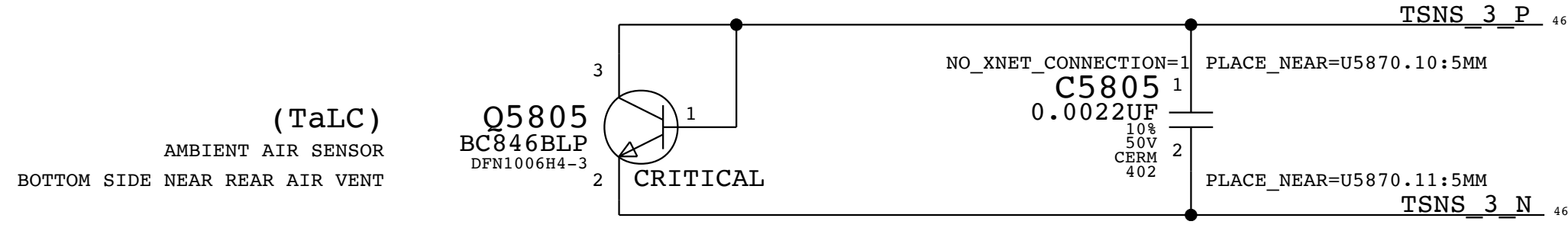
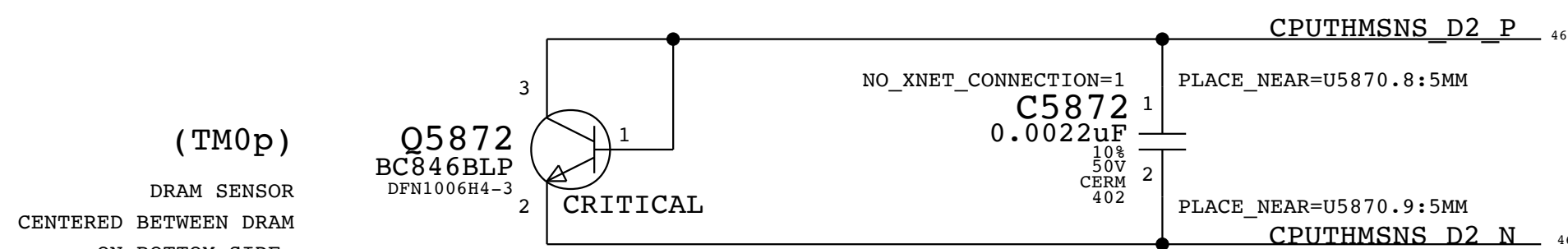
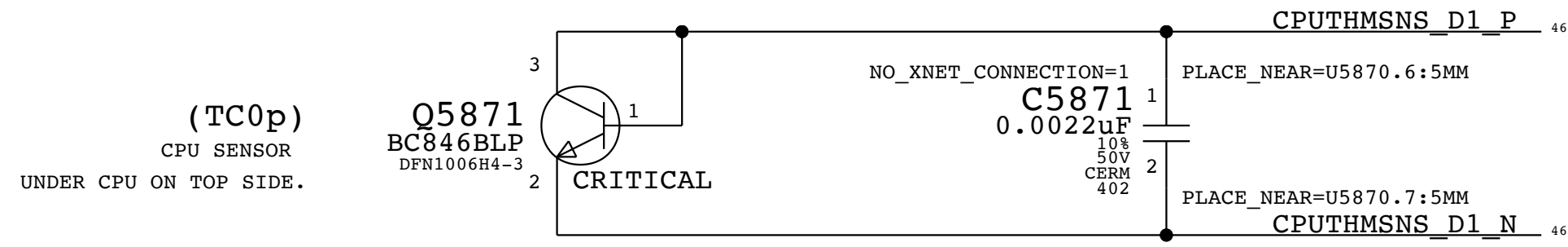
2

1




Thermal Sensor B & CPU High Peak Detection:  
CPU Proximity, Memory Proximity, Airflow, Fin Stack Proximity

I2C Write: 0x98, I2C Read: 0x99



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qq群 : 241000

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BOM\_COST\_GROUP=SENSORS

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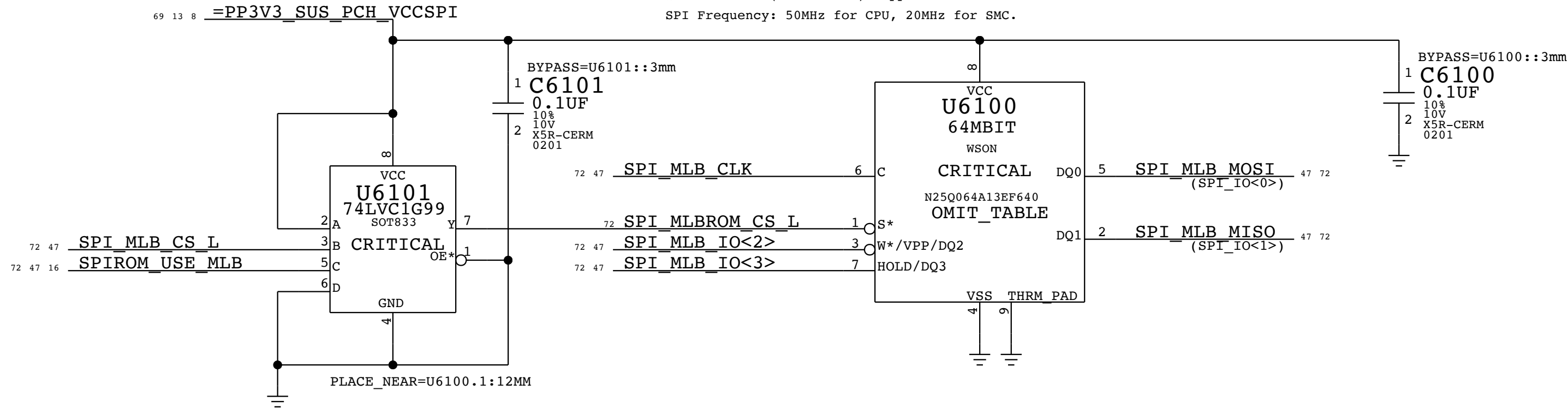
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SPI ROM - Combo BGA Footprint (3 vendors)

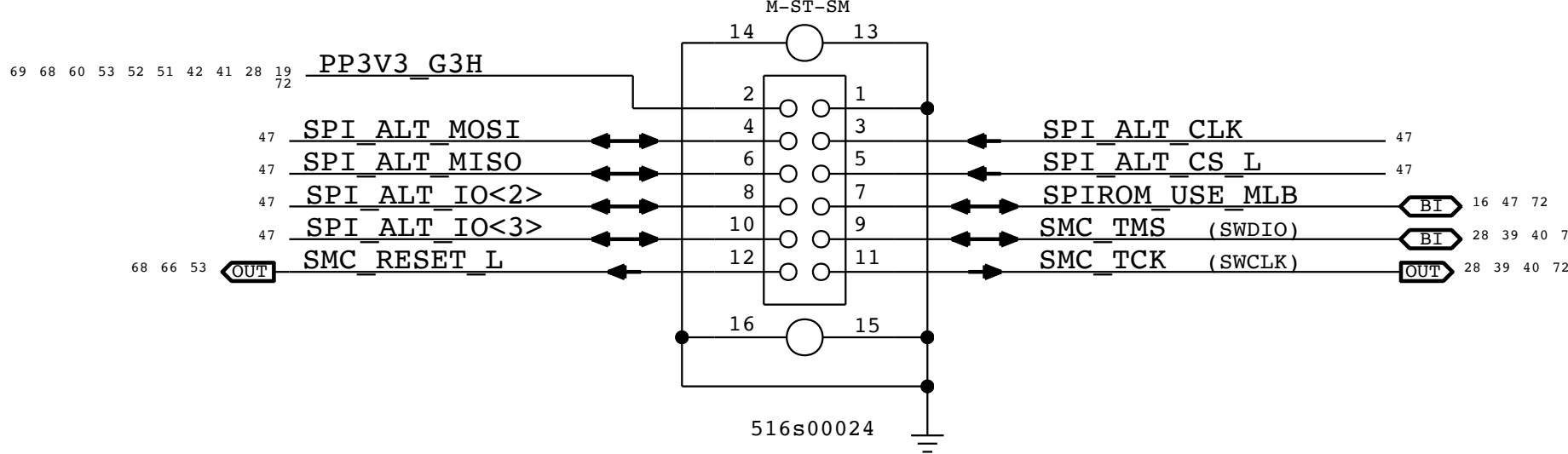
Quad-IO Mode (Mode 0 & 3) supported.  
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



SPI+SWD SAM Connector

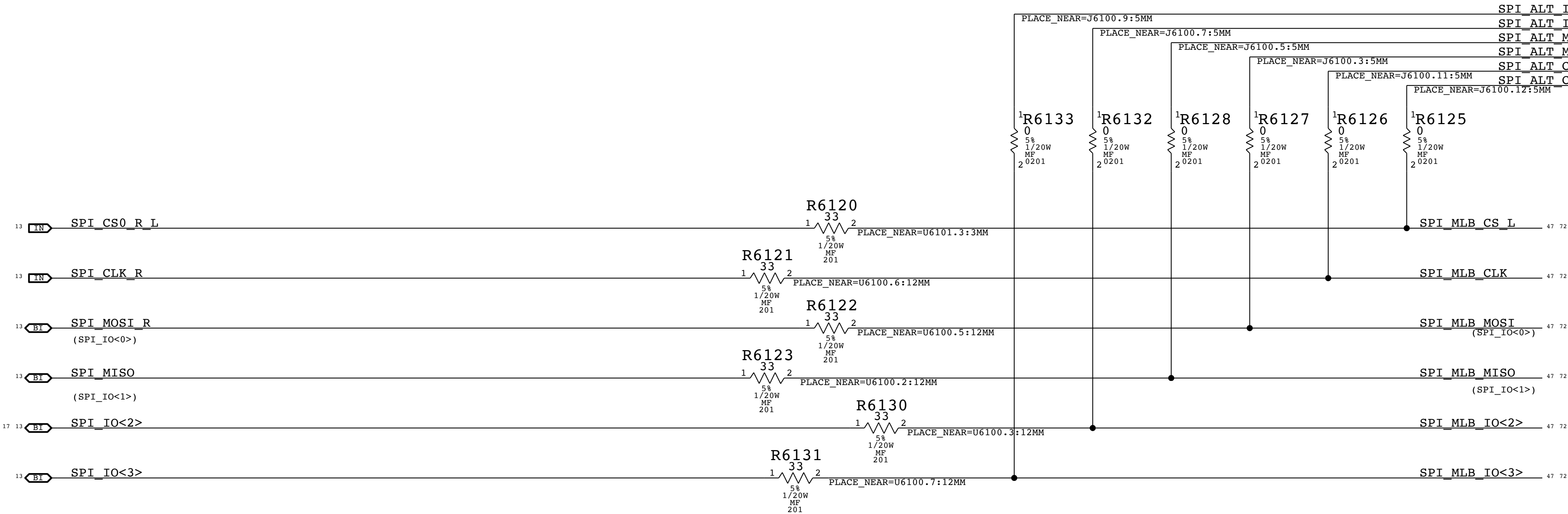
CRITICAL

J6100  
DF40PC-12DP-0.4V-51  
M-SMT-SW



BootROM SPI Bus Series Termination

CPU Master




Sam Card ROM Slave

SPI ROM Slave

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BOM\_COST\_GROUP=CPU SUPPORT

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SPI ROM & SWD Debug		
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BOM\_COST\_GROUP=CPU SUPPORT

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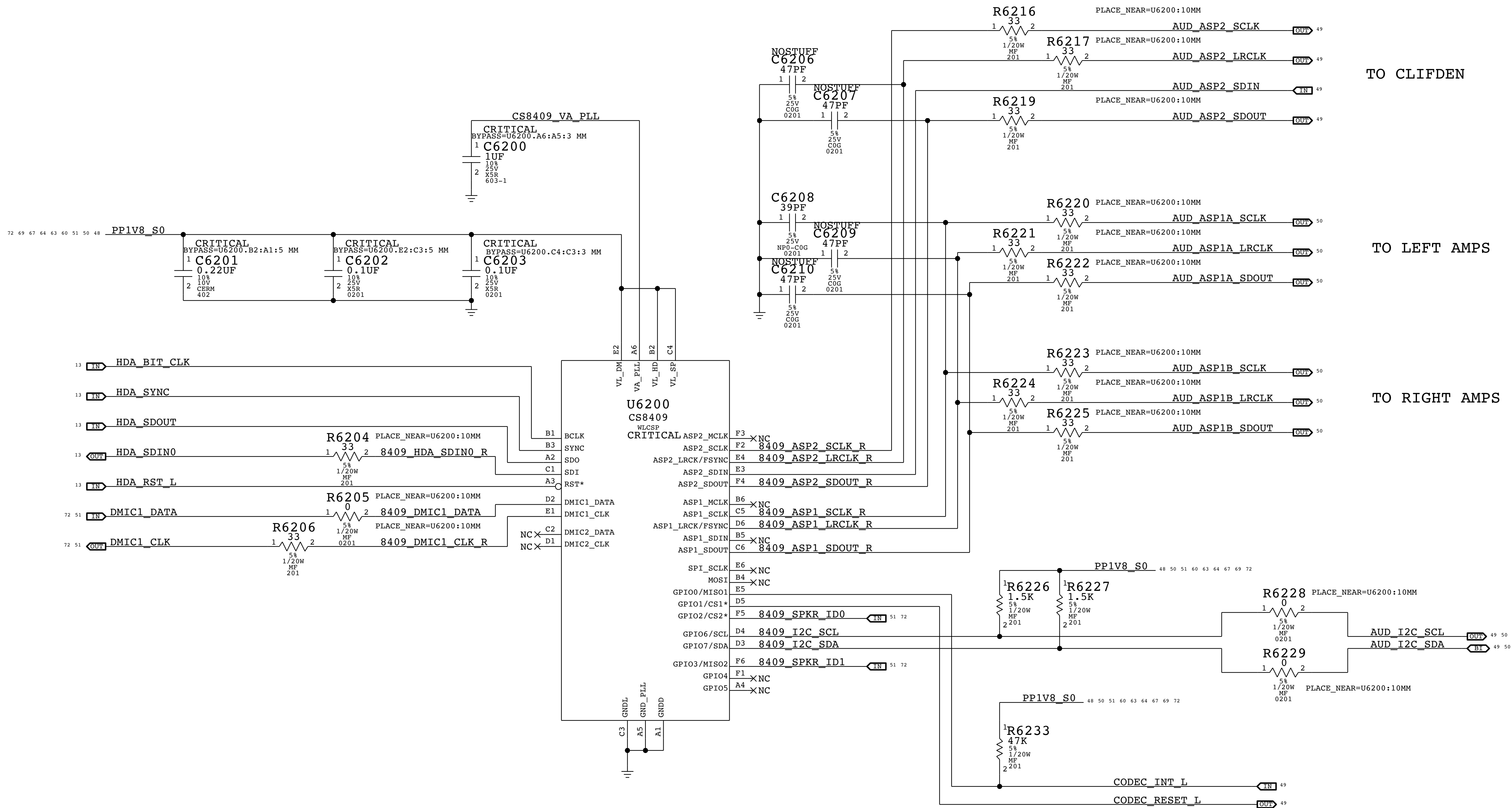
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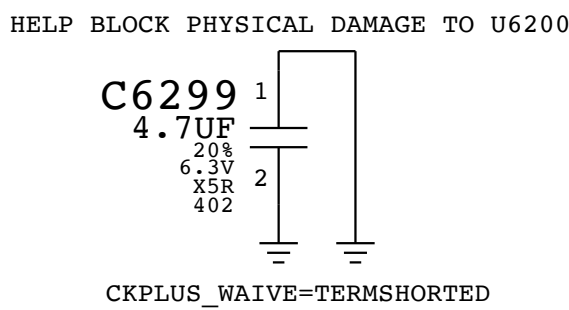
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qq群 : 241000

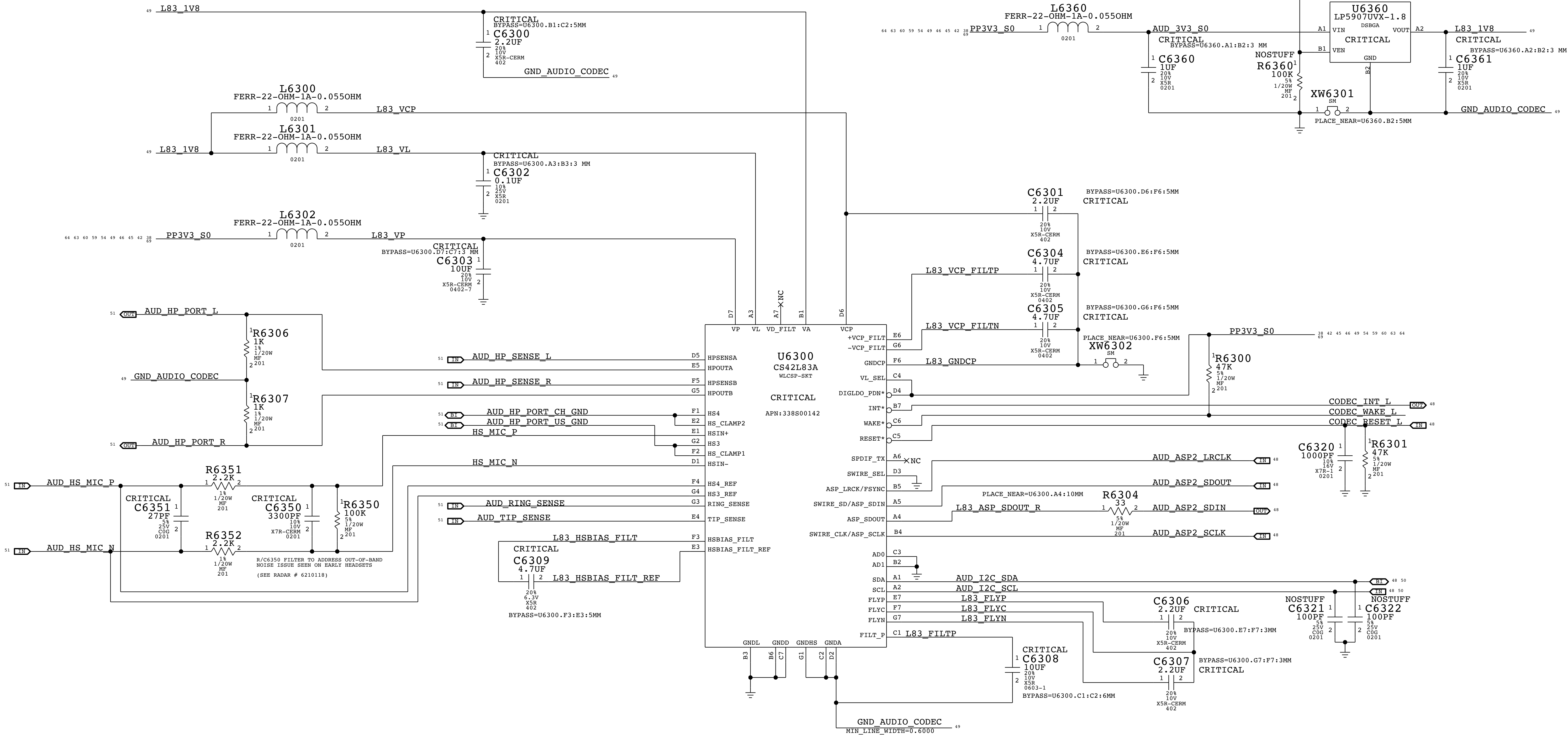


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HDA BRIDGE			
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AD1 AD0 I2C ADDR  
GND GND 0X48 <--  
GND 1.8V 0X49  
1.8V GND 0X4A  
1.8V 1.8V 0X4B



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BOM\_COST\_GROUP=AUDIO

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4X MONO SPEAKER AMPLIFIERS

APN: 353S00685  
GAIN: 0DBFS = 7VRMS

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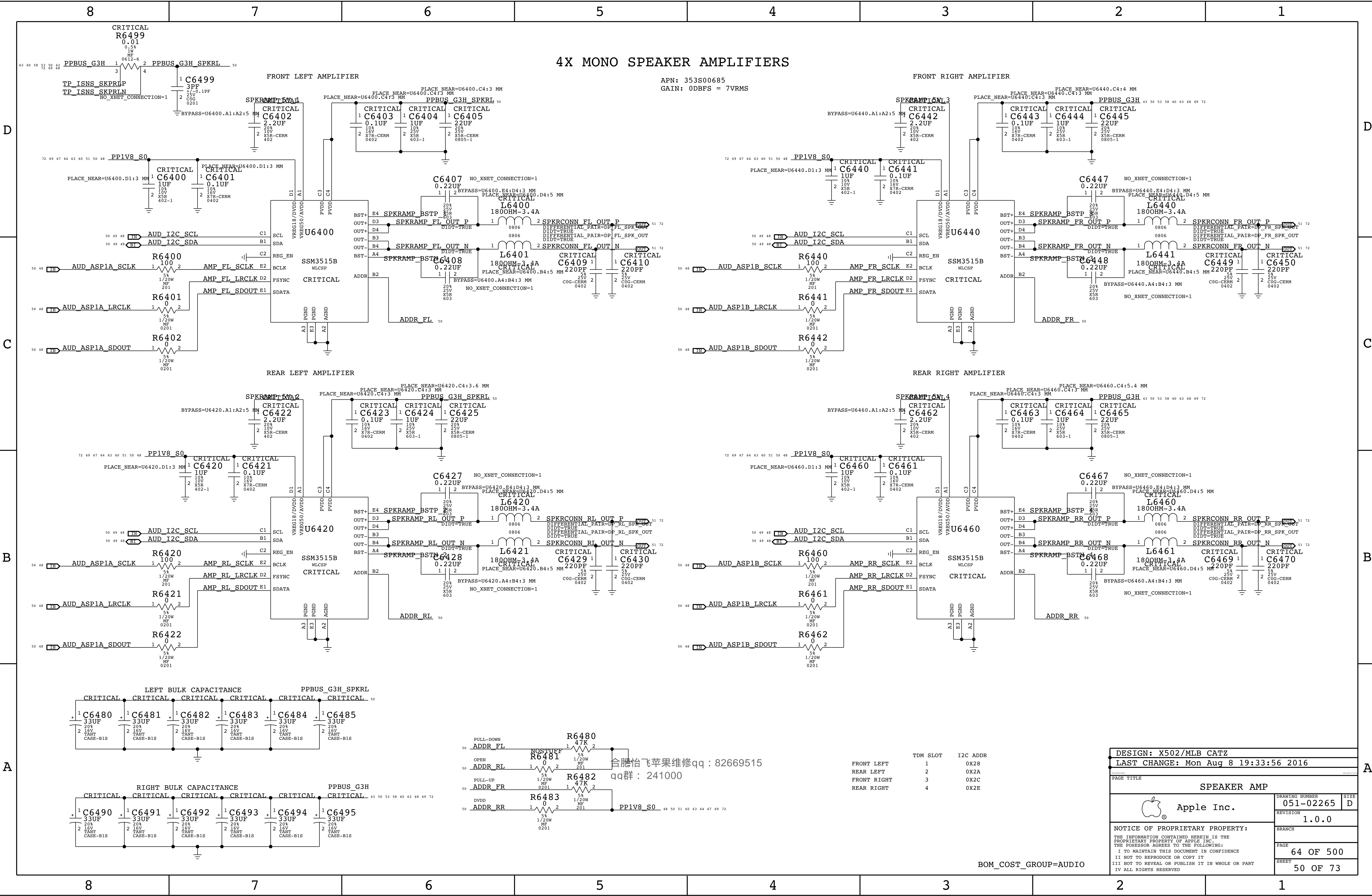
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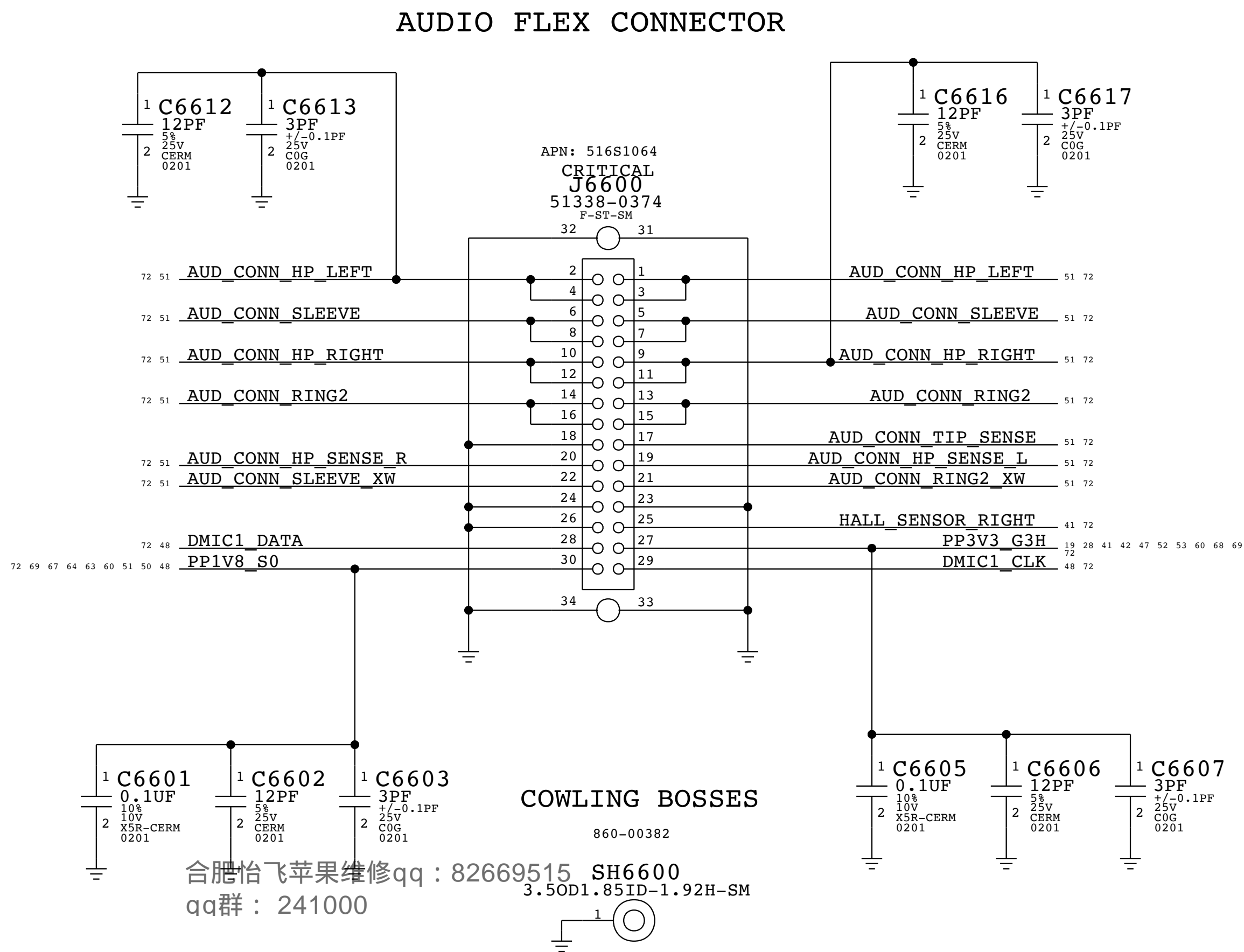
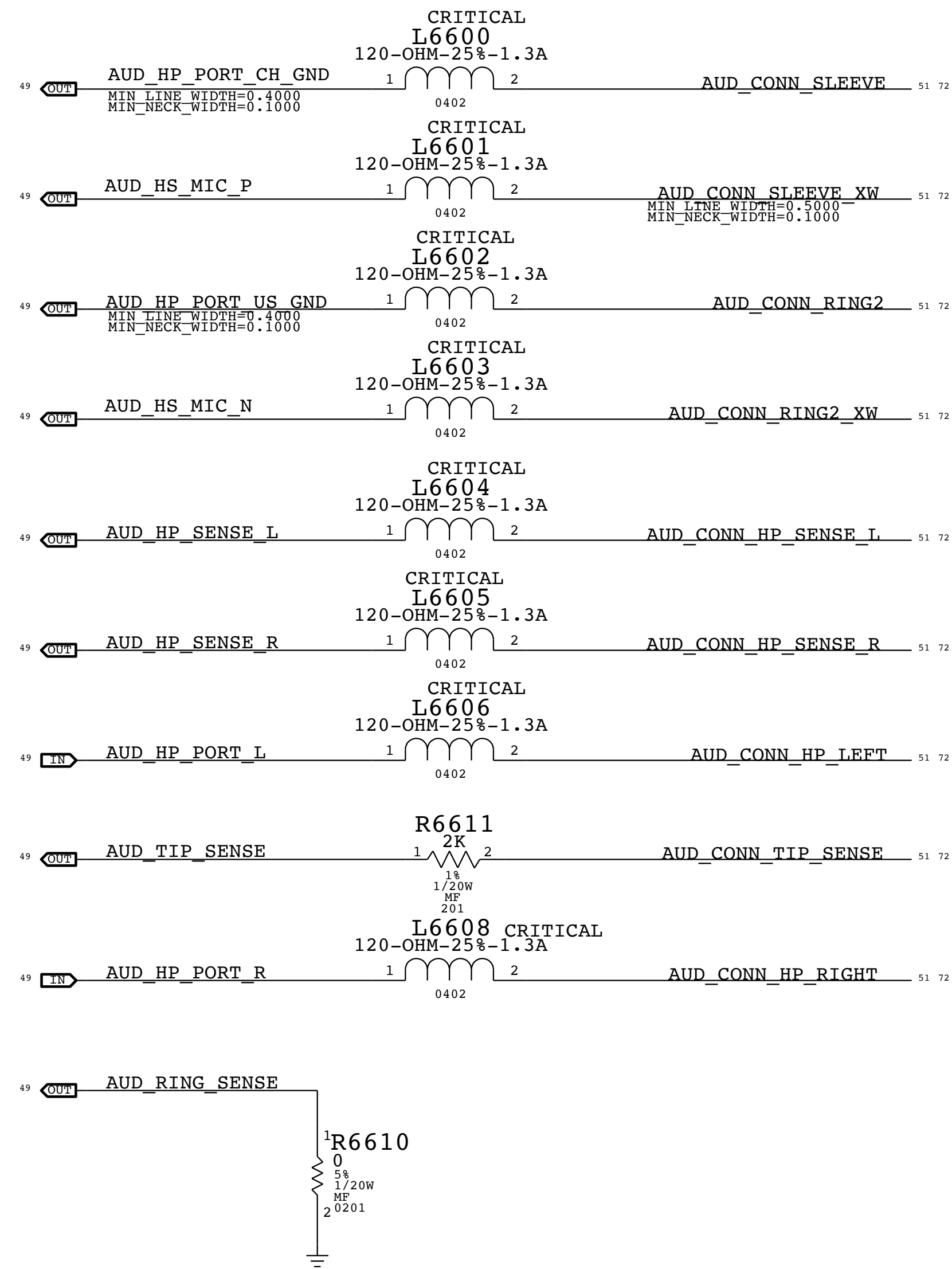
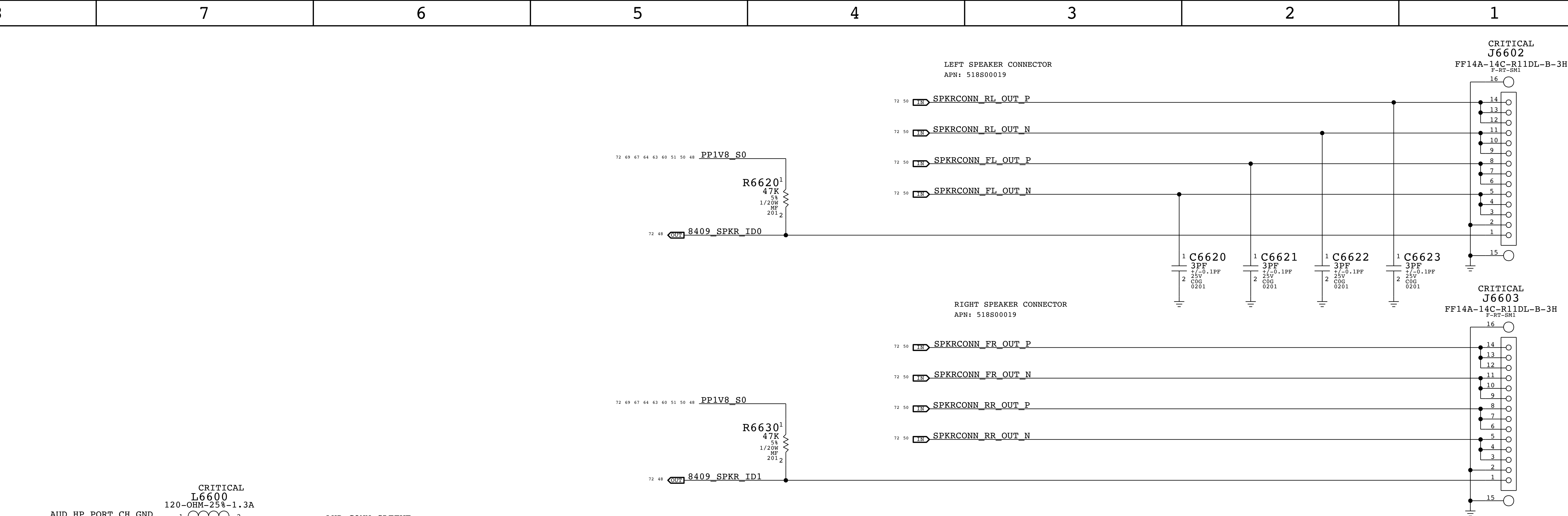
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BOM\_COST\_GROUP=AUDIO

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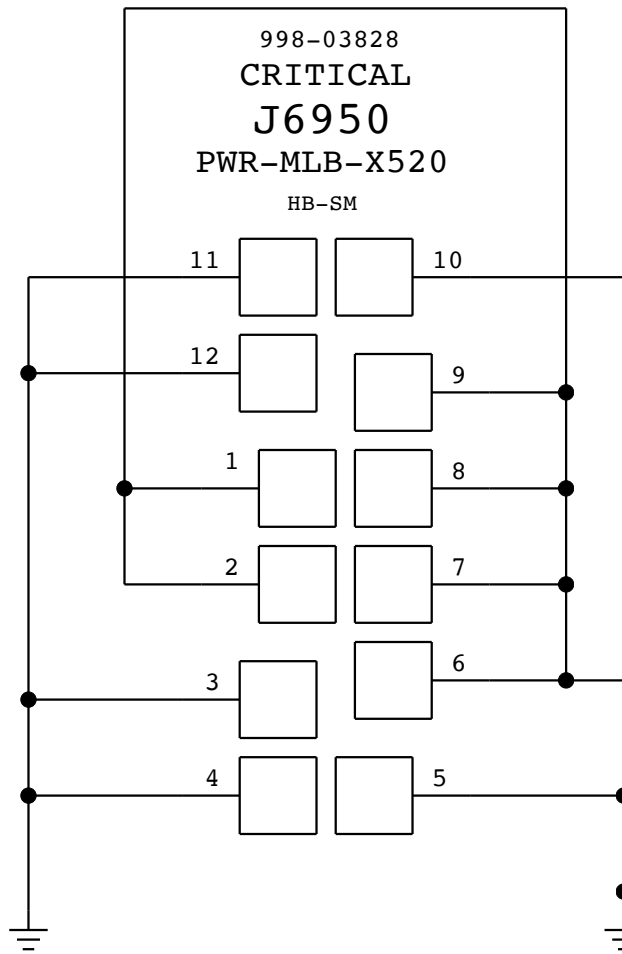
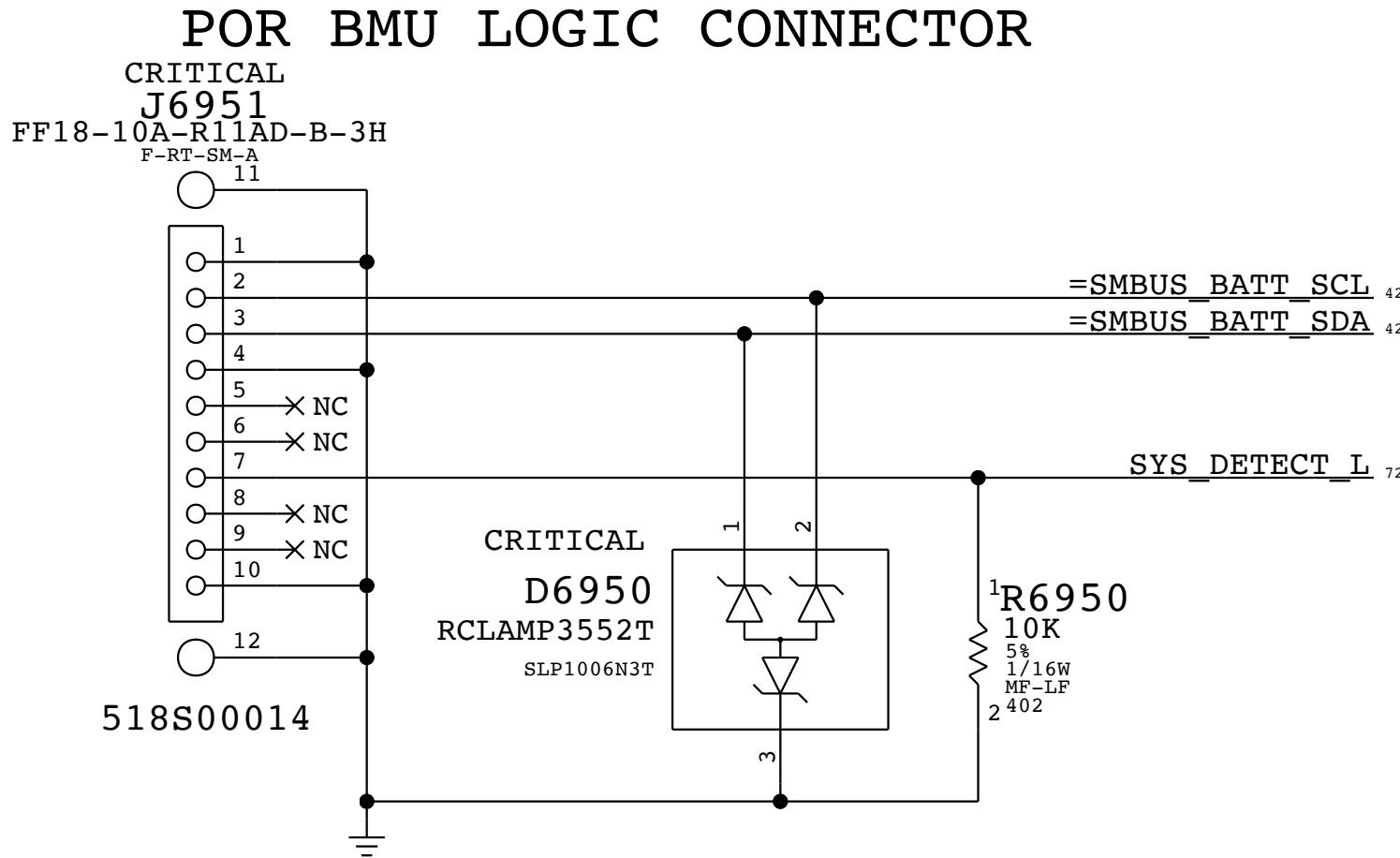
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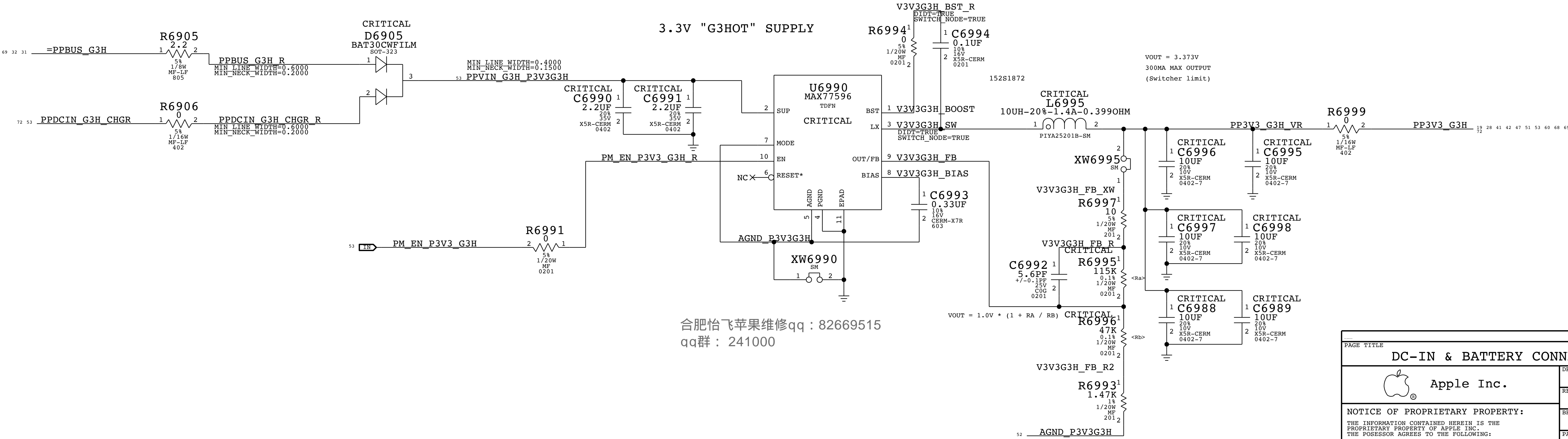
A

POR BATTERY (BMU) FLEX SOLDER PADS.



BMU power flex is soldered to MLB.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	



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DC-IN & BATTERY CONNECTORS		
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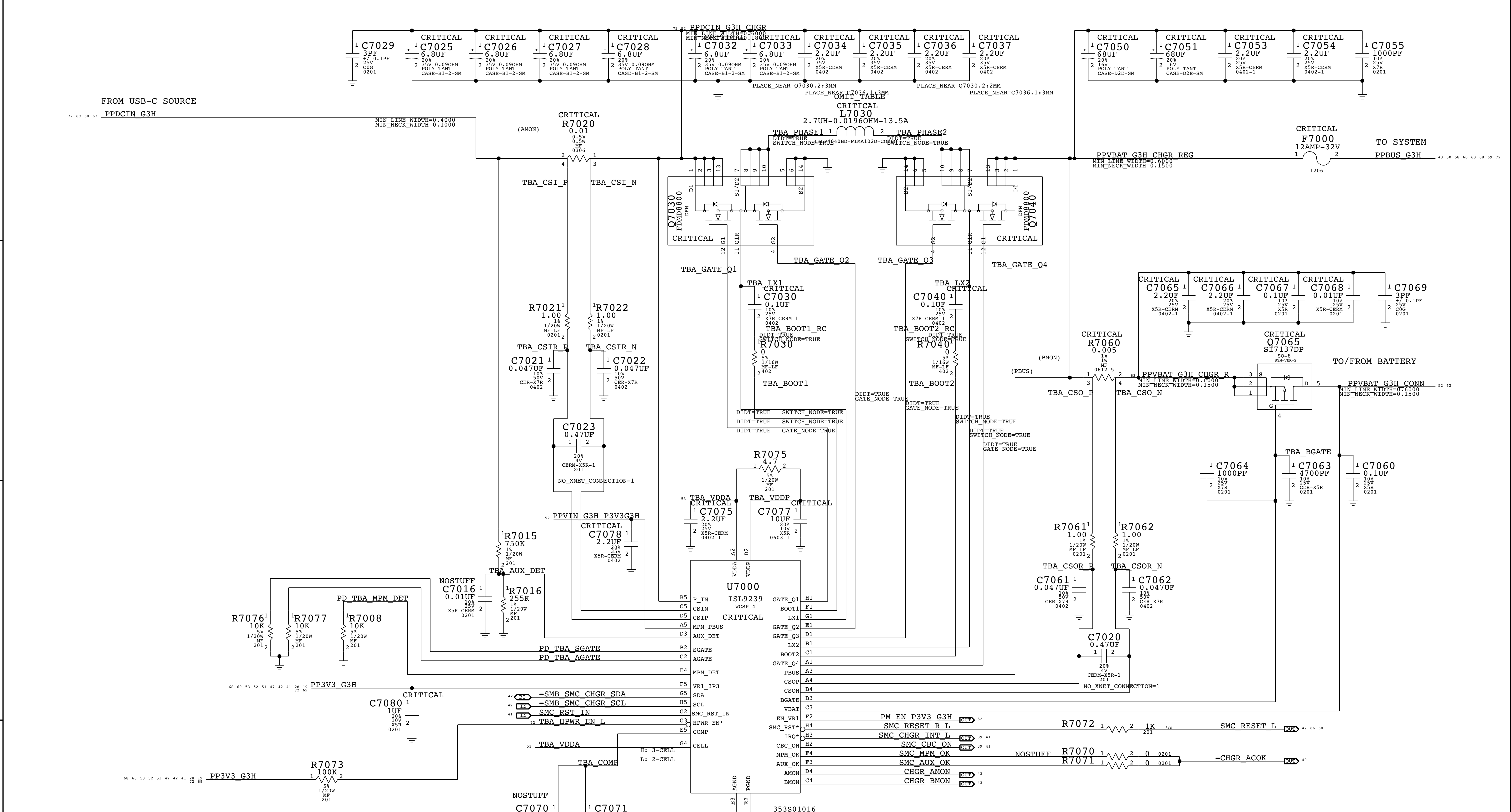
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

BOM\_COST\_GROUP=PLATFORM POWER

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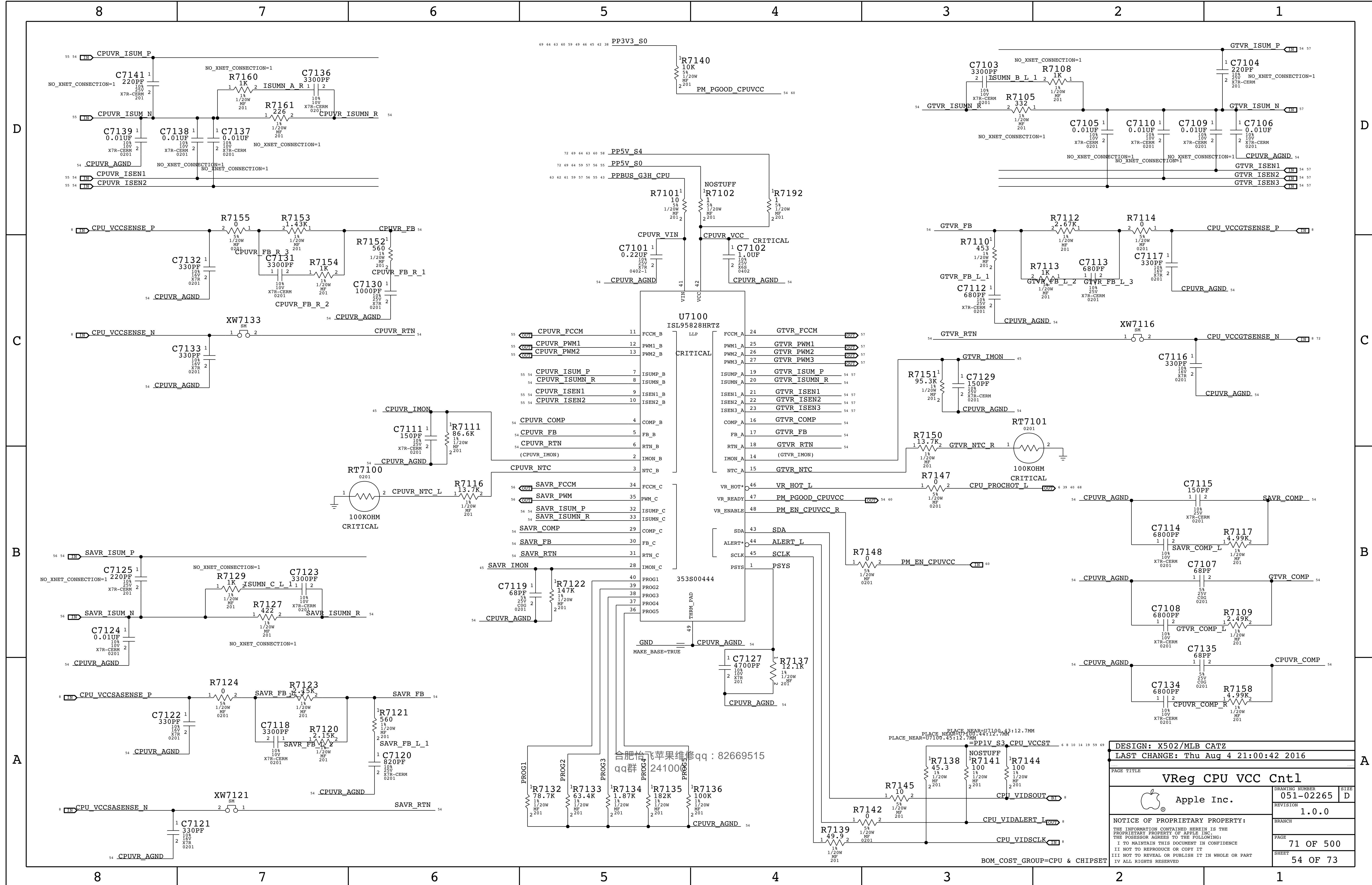
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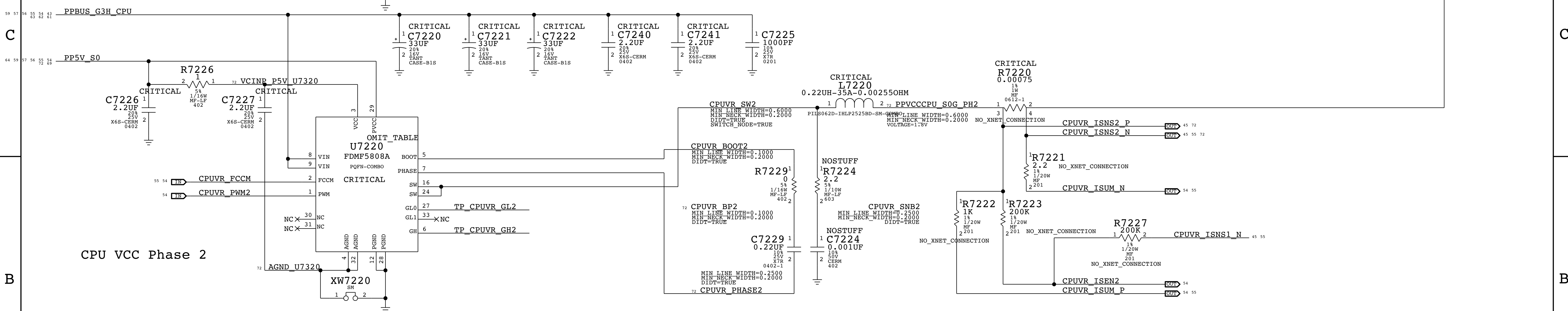
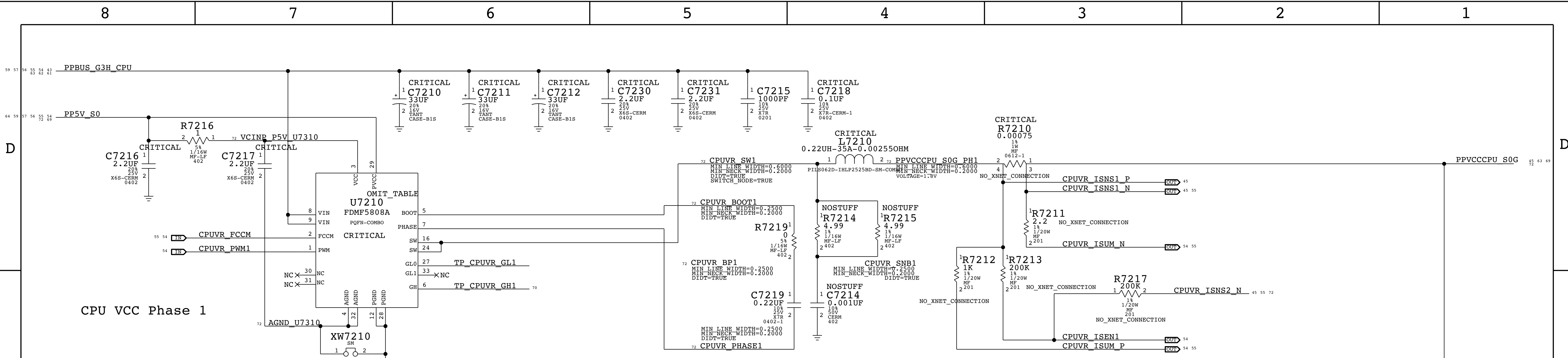
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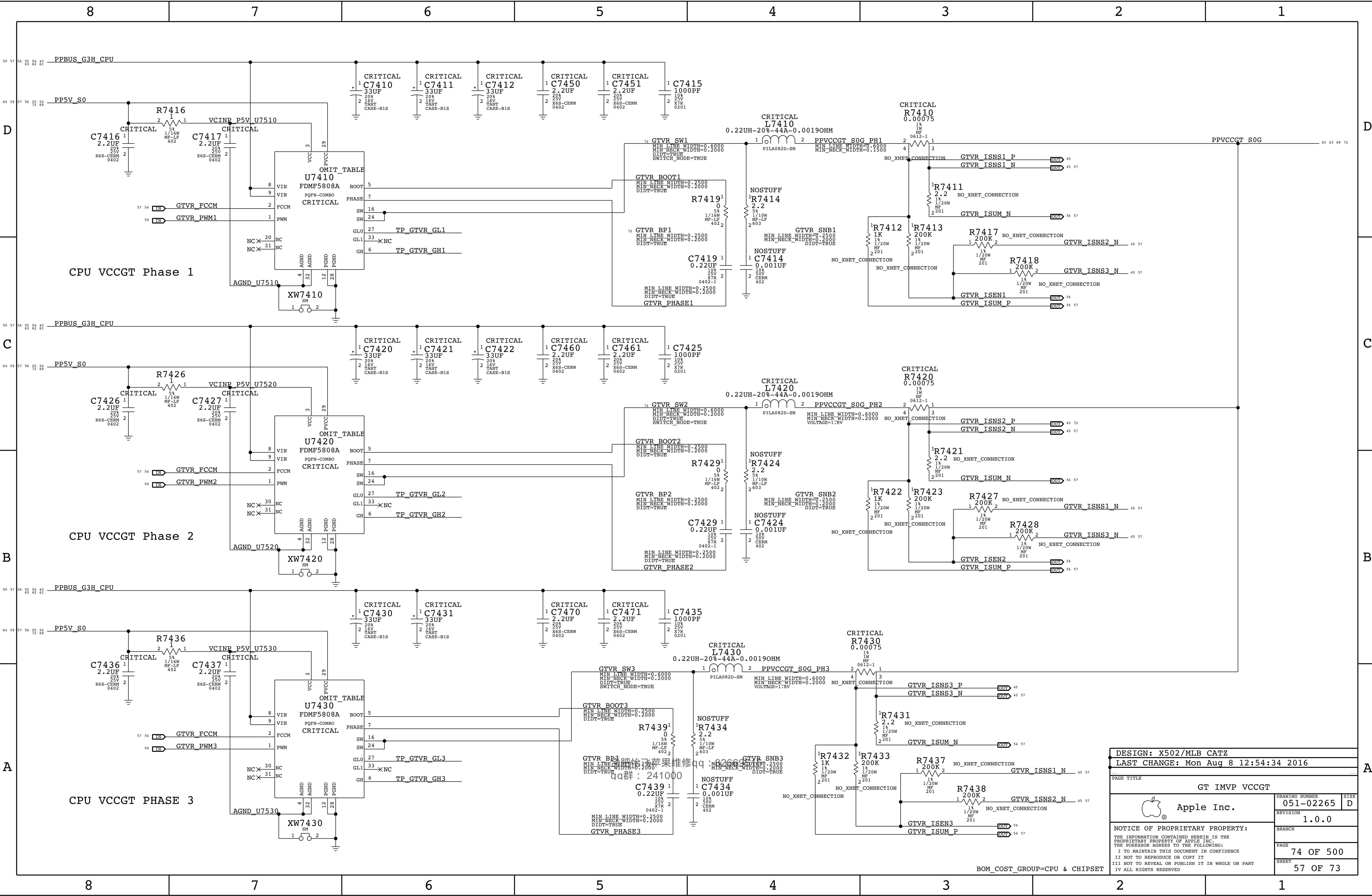
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353S00497	5	IC, SIC635, DR MOS, IMVP-8, 40A, PQFN31, 5X5	U7210, U7220, U7410, U7420, U7430	CRITICAL	


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CPU IMVP VCC & VCCSA		
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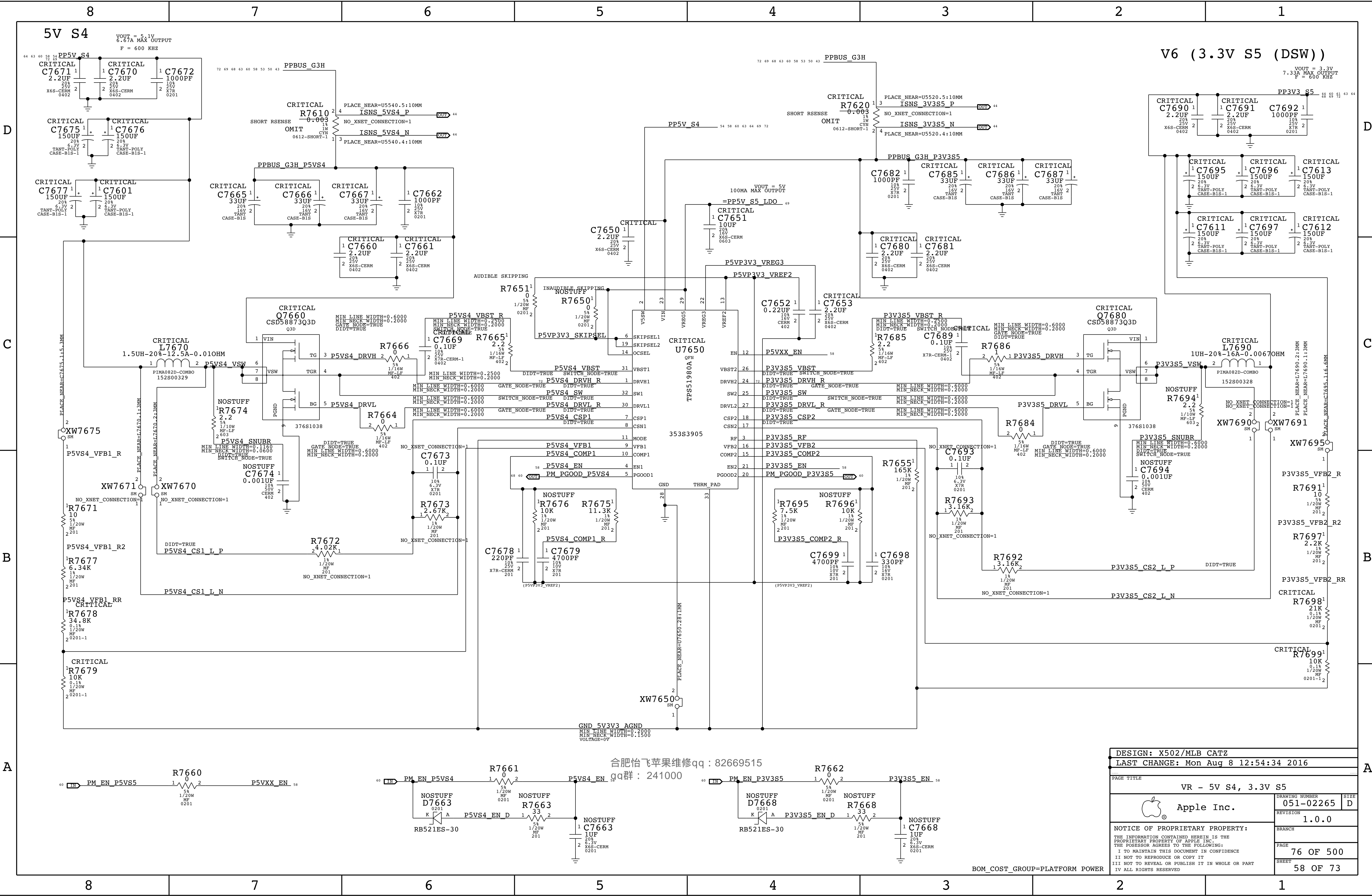




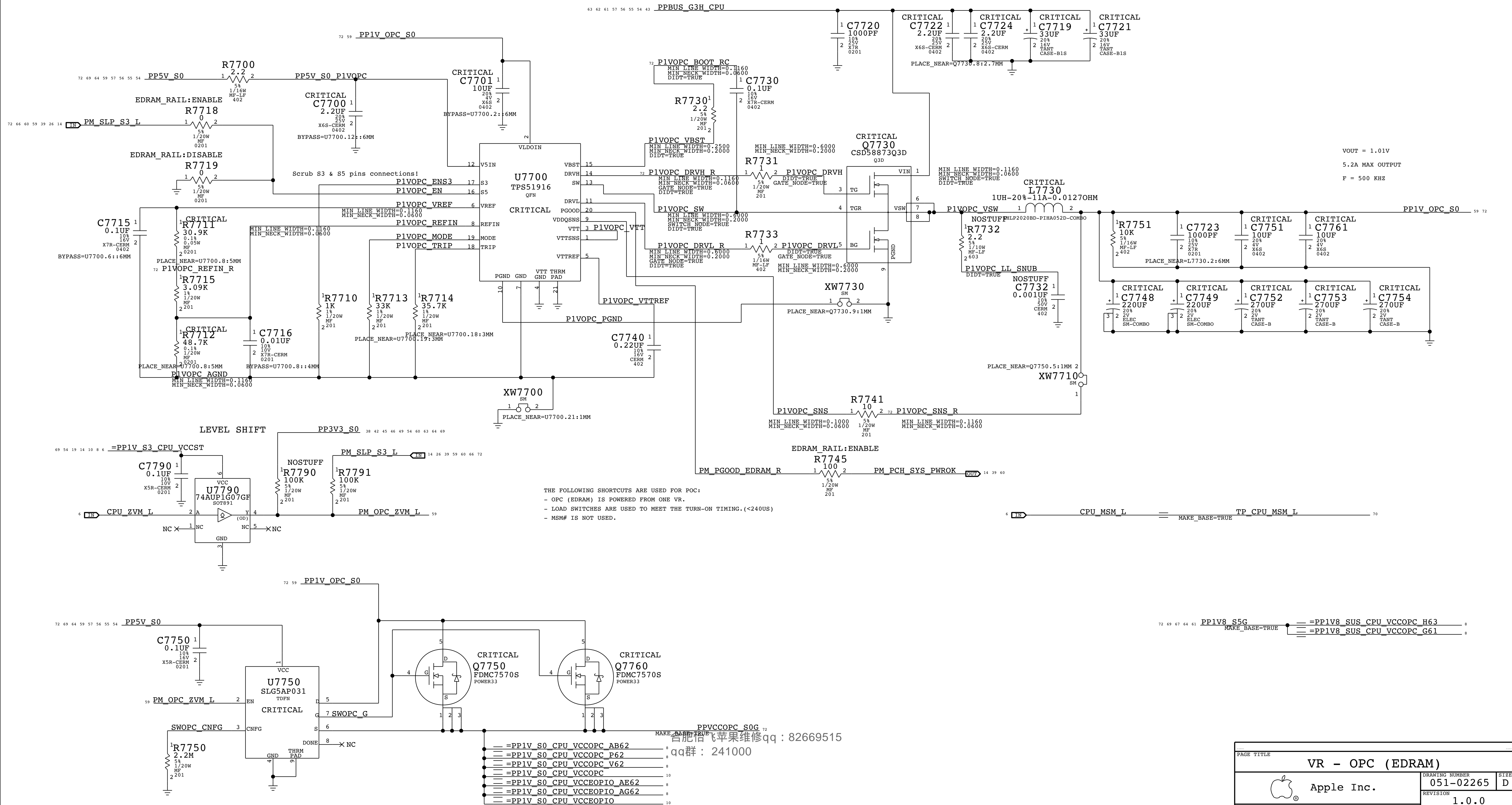


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GT IMVP VCCGT		
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BOM\_COST\_GROUP=CPU & CHIPSET




1V S0 REGULATOR FOR EDRAM (ON-PACKAGE CACHE)



THE FOLLOWING SHORTCUTS ARE USED FOR POC:  
- OPC (EDRAM) IS POWERED FROM ONE VR.  
- LOAD SWITCHES ARE USED TO MEET THE TURN-ON TIMING. (<240US)  
- MSM# IS NOT USED.

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VR - OPC (EDRAM)		
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BOM\_COST\_GROUP=CPU & CHIPSET







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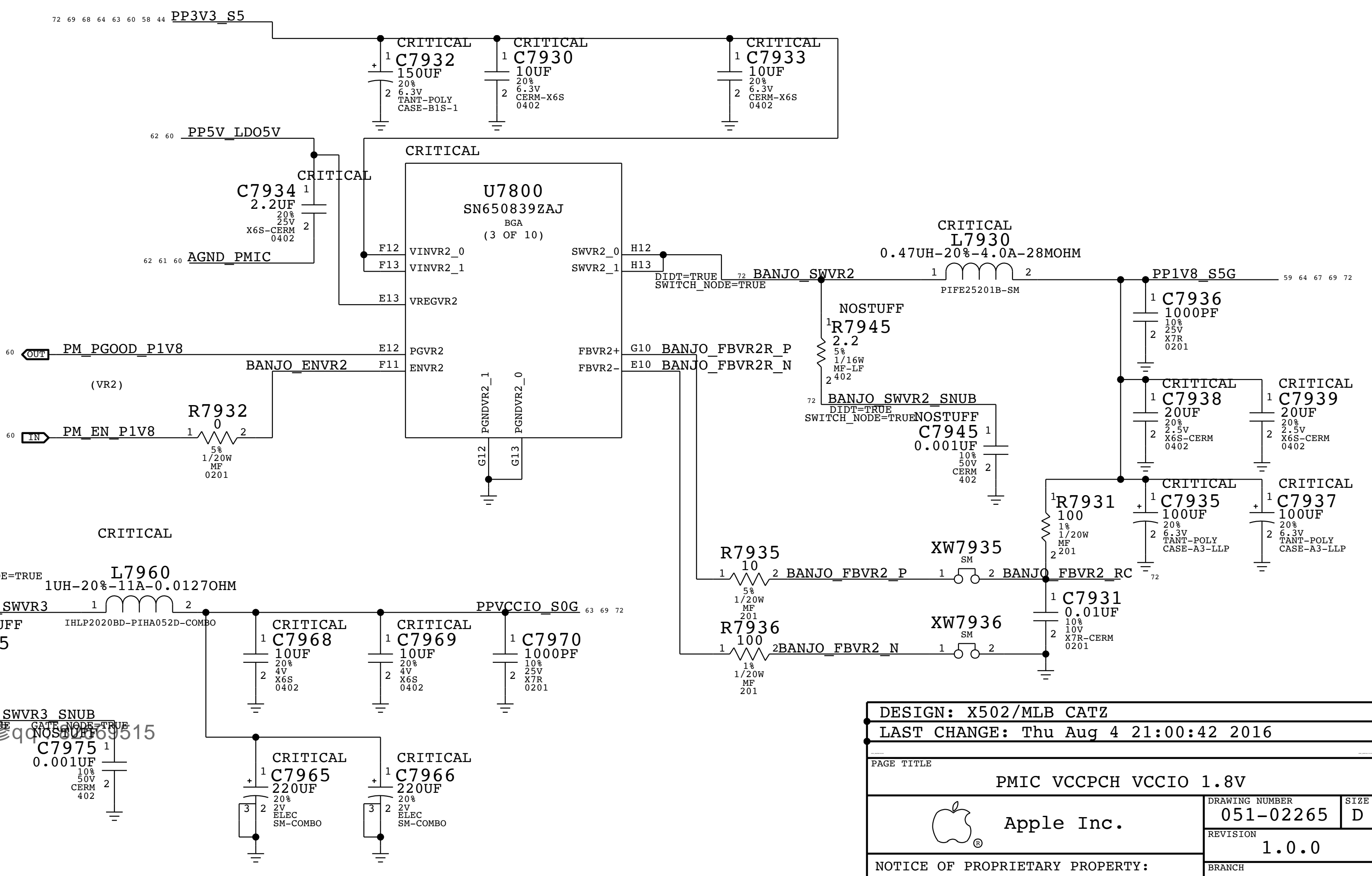
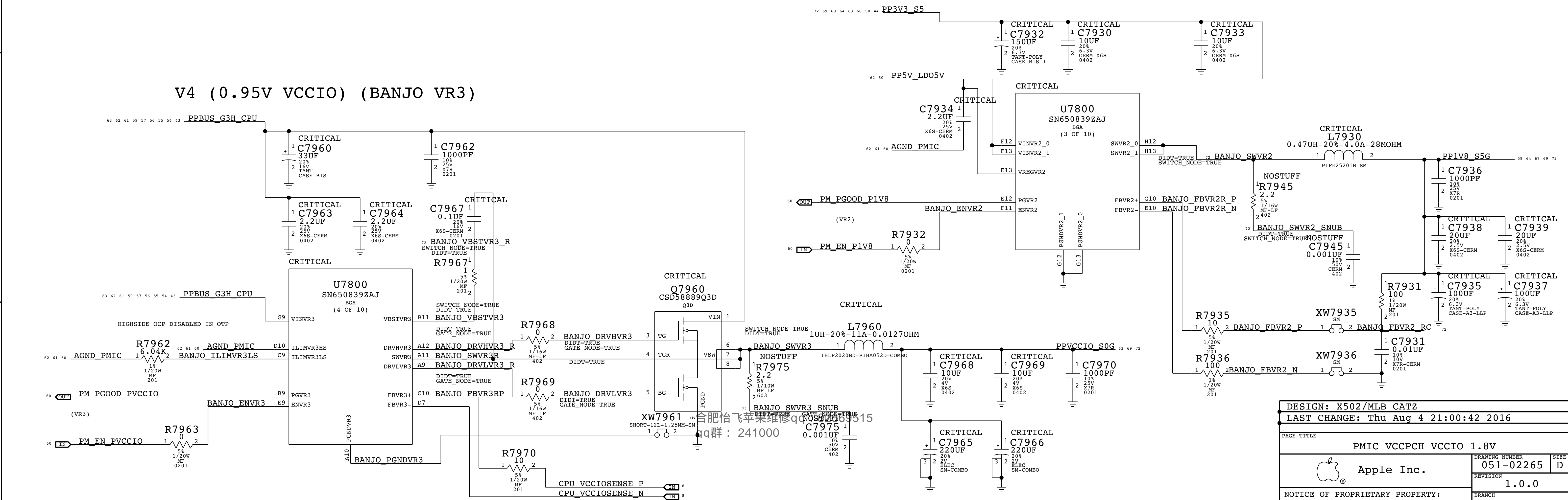
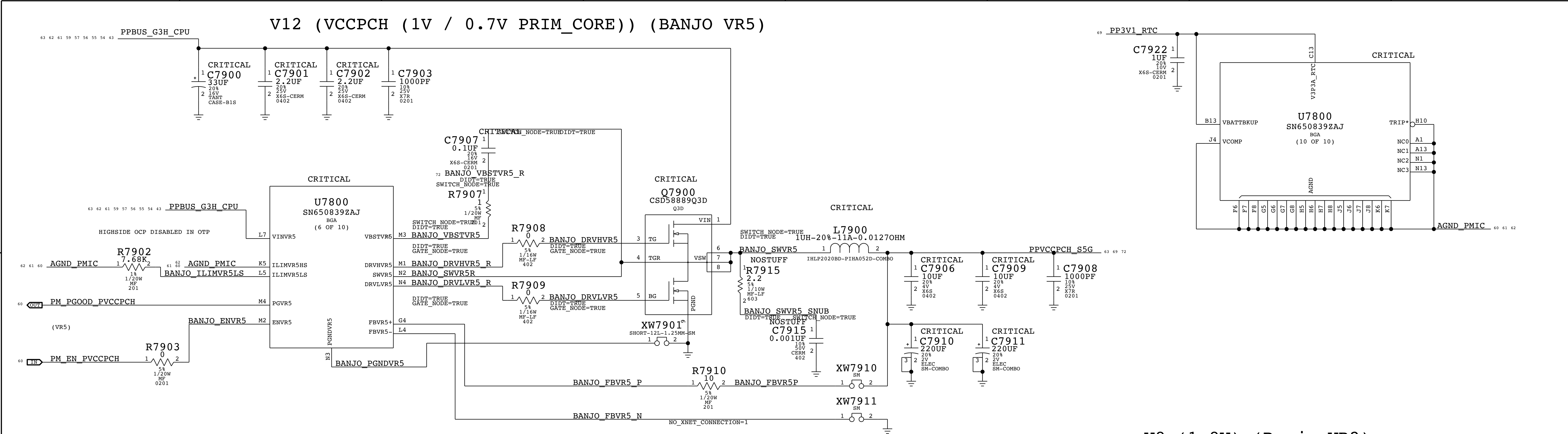
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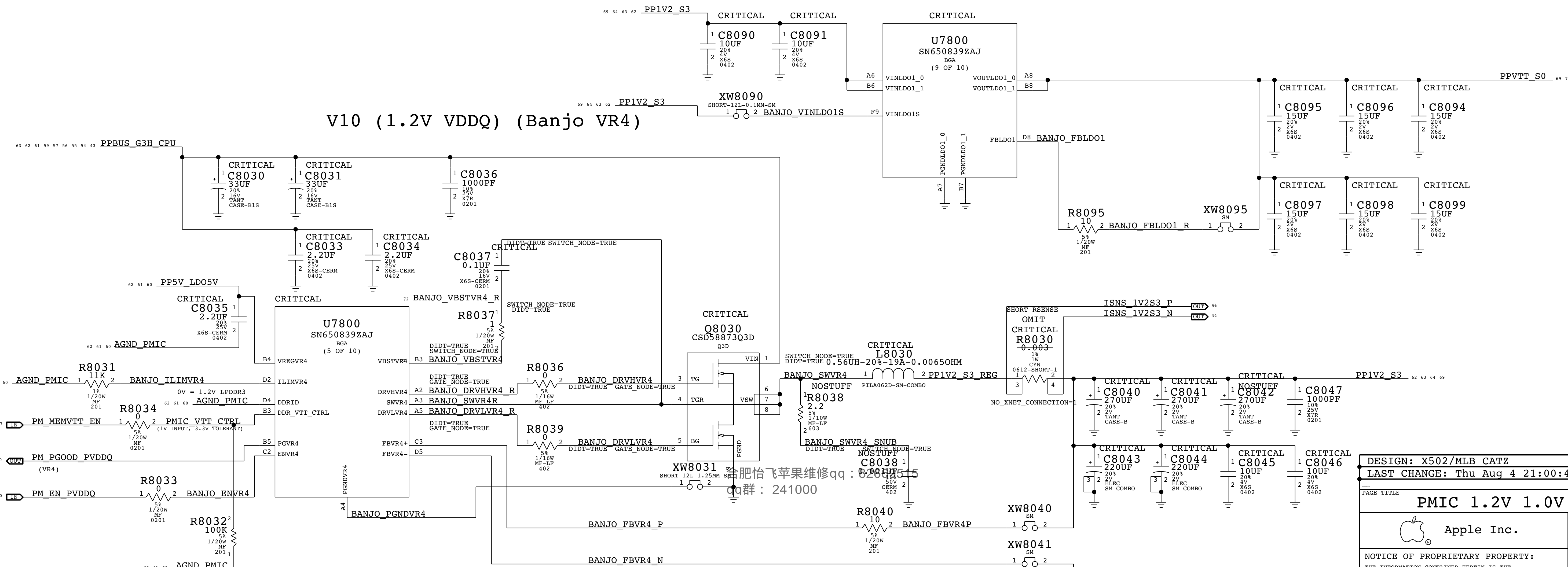
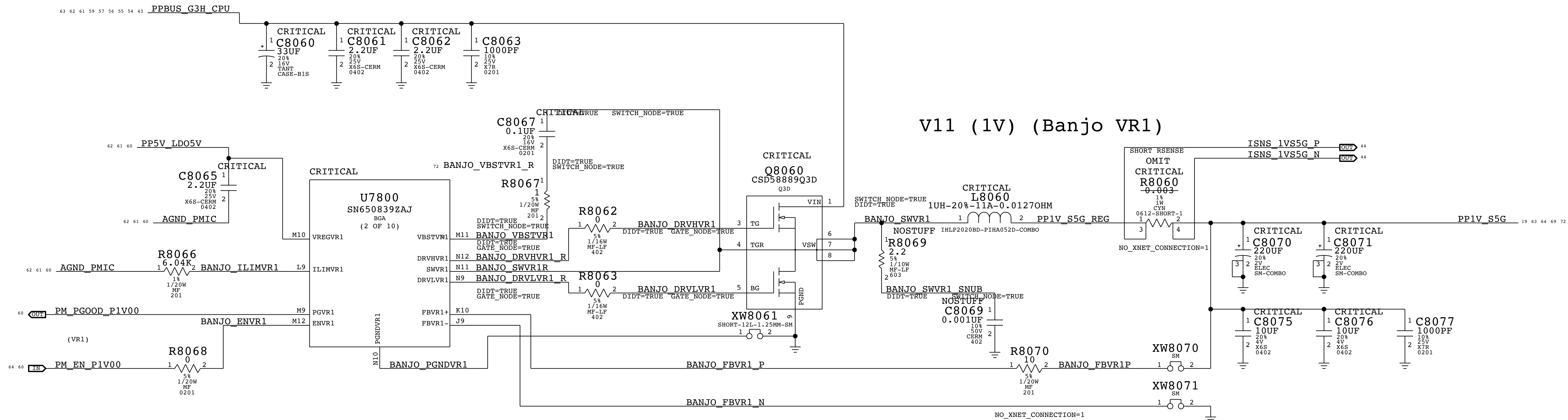
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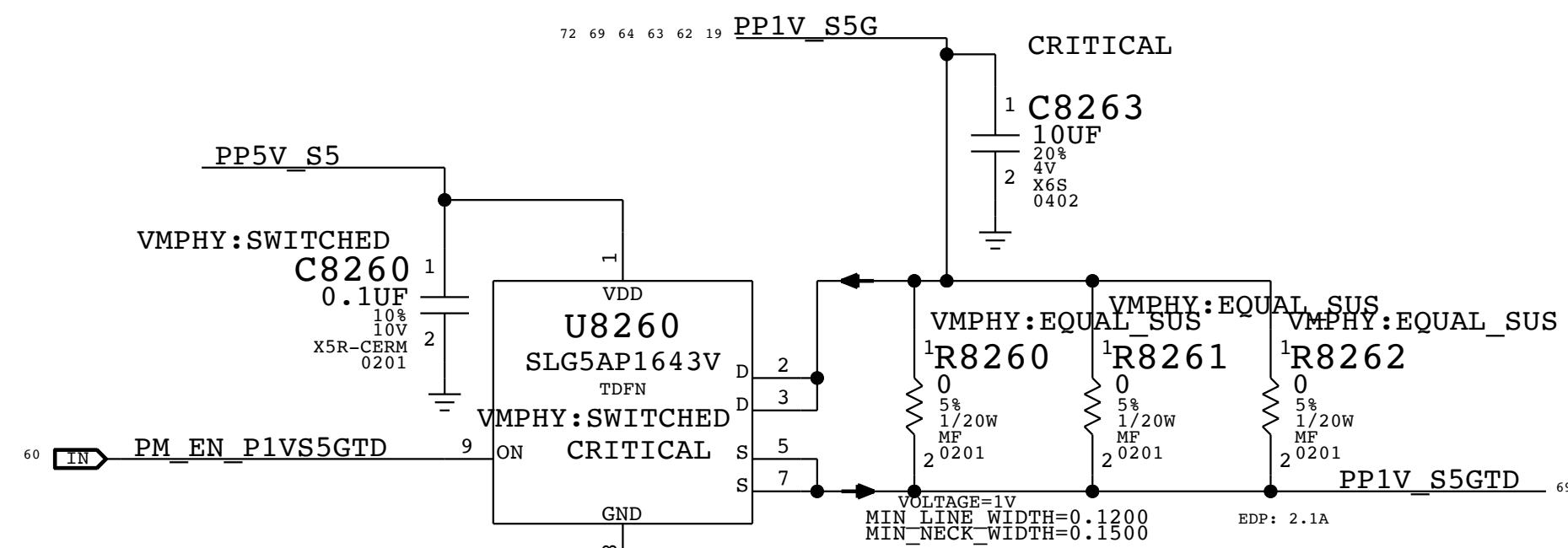
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BOM\_COST\_GROUP=PLATFORM POWER



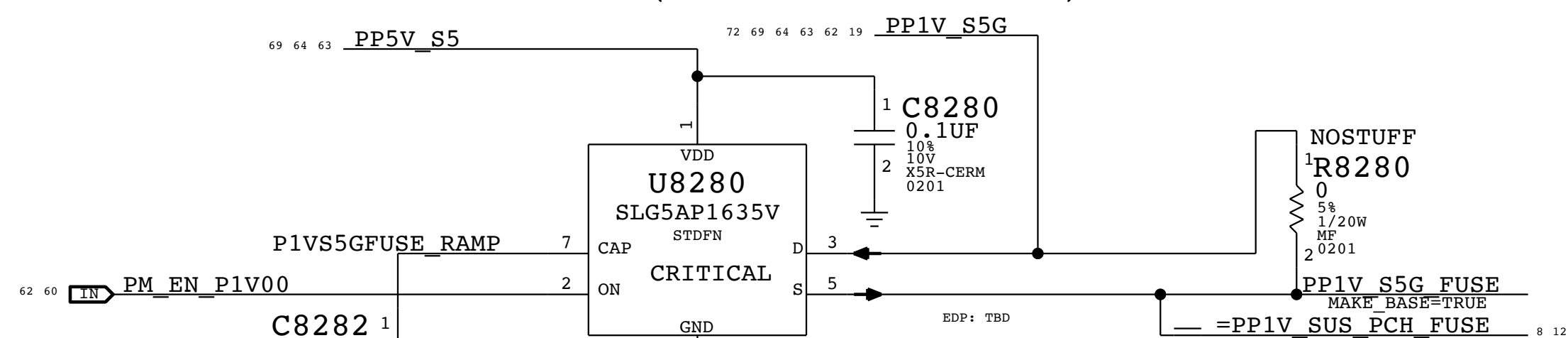
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PAGE TITLE			
PMIC 1.2V 1.0V 0.6V			
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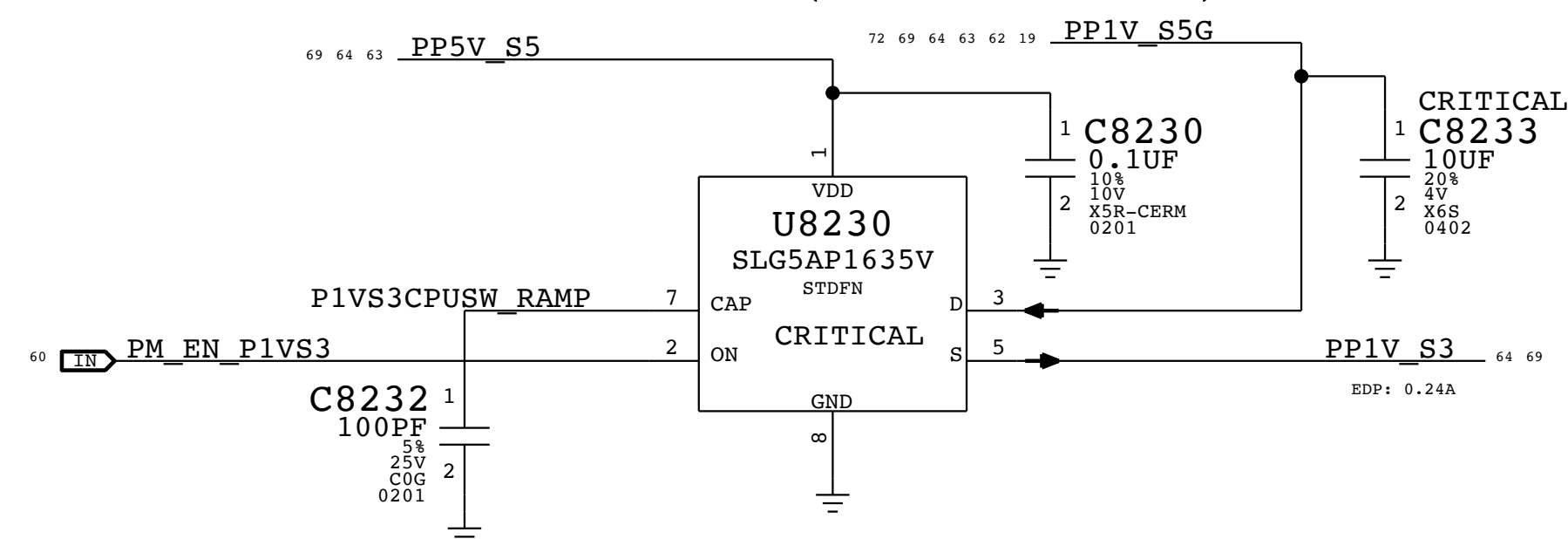
Part	SLG5AP1643V
Type	Load Switch
R(on) @ 25C	7.4 MOHM TYP
R(on) @ 70C	10.6 MOHM MAX
Current	6A MAX
TON-TOTAL	65US MAX @ 1V

1V S5G FUSE (FOR FAST TURN OFF)



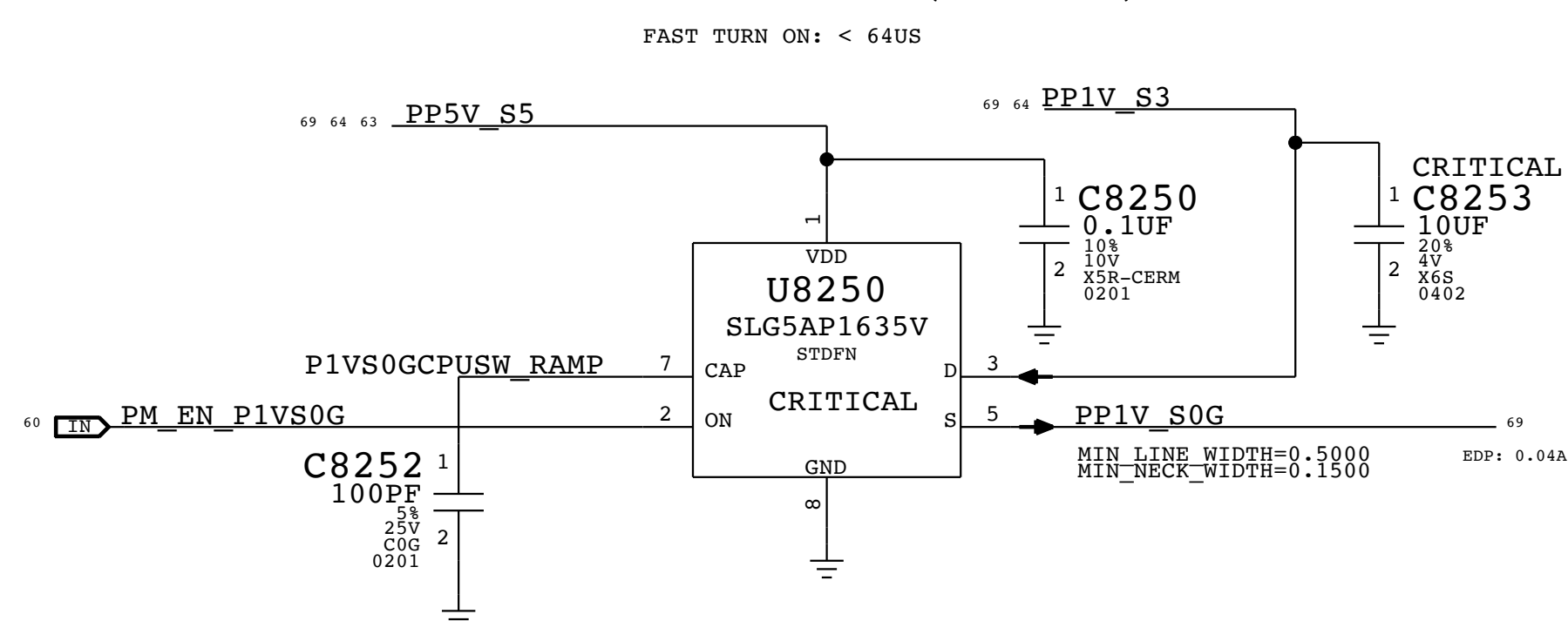
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

1V S3 SWITCH (VCCST, VCCPLL)



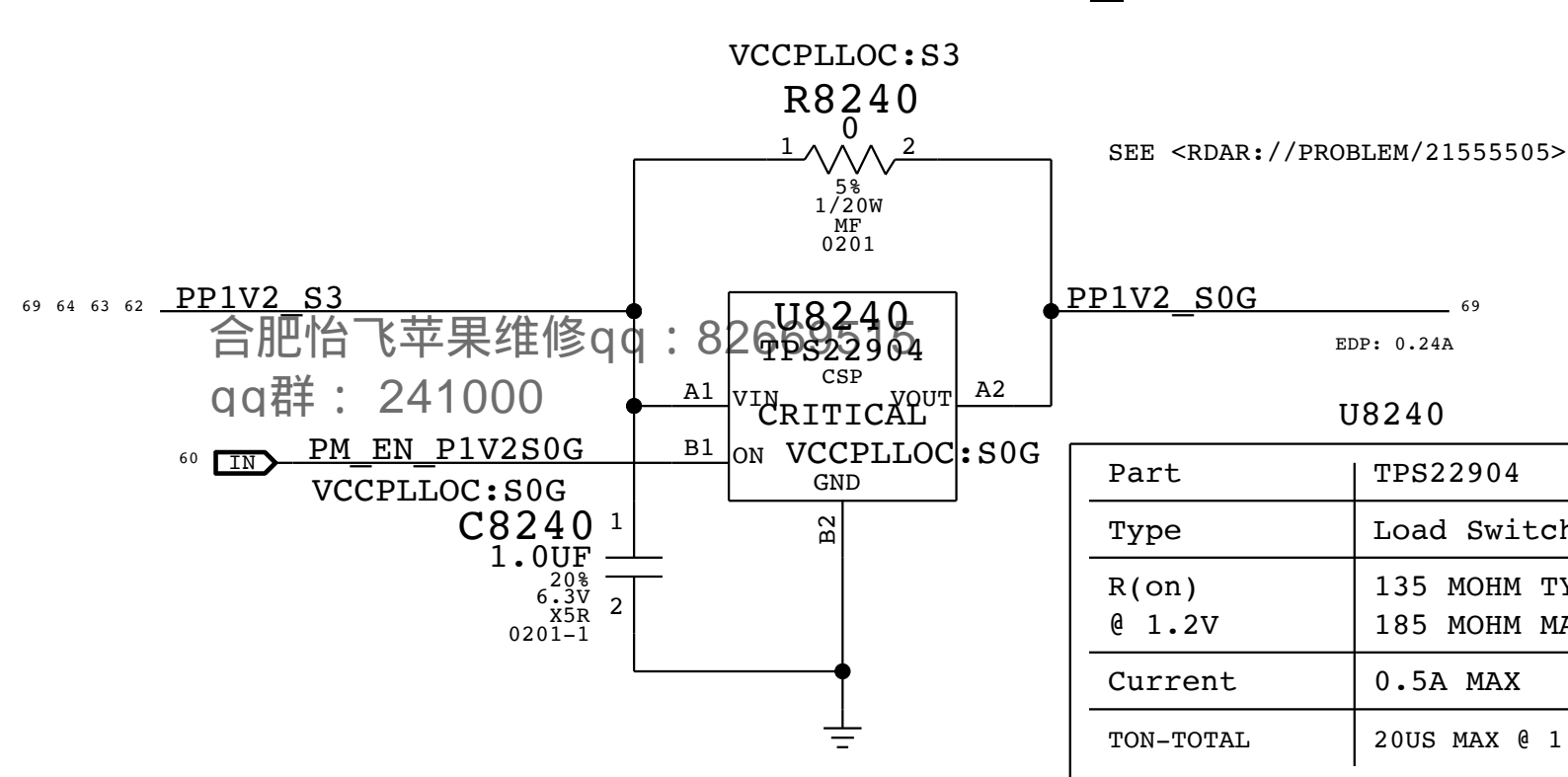
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

## 1V S0G CPU SWITCH (VCCSTG)

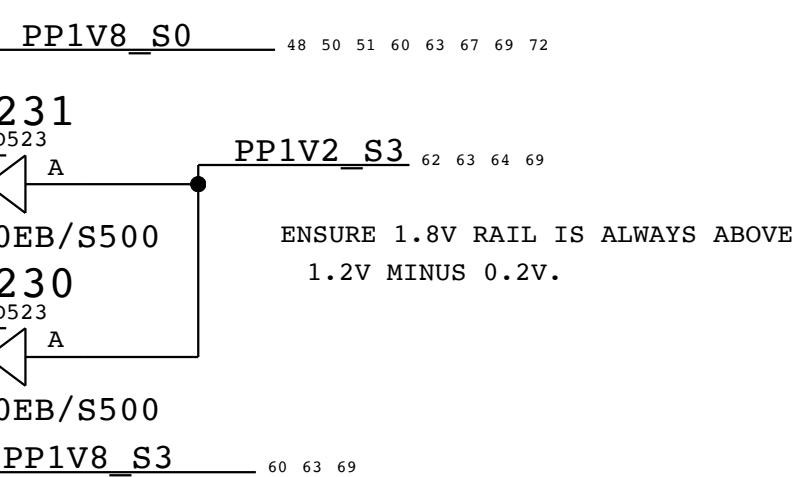


Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

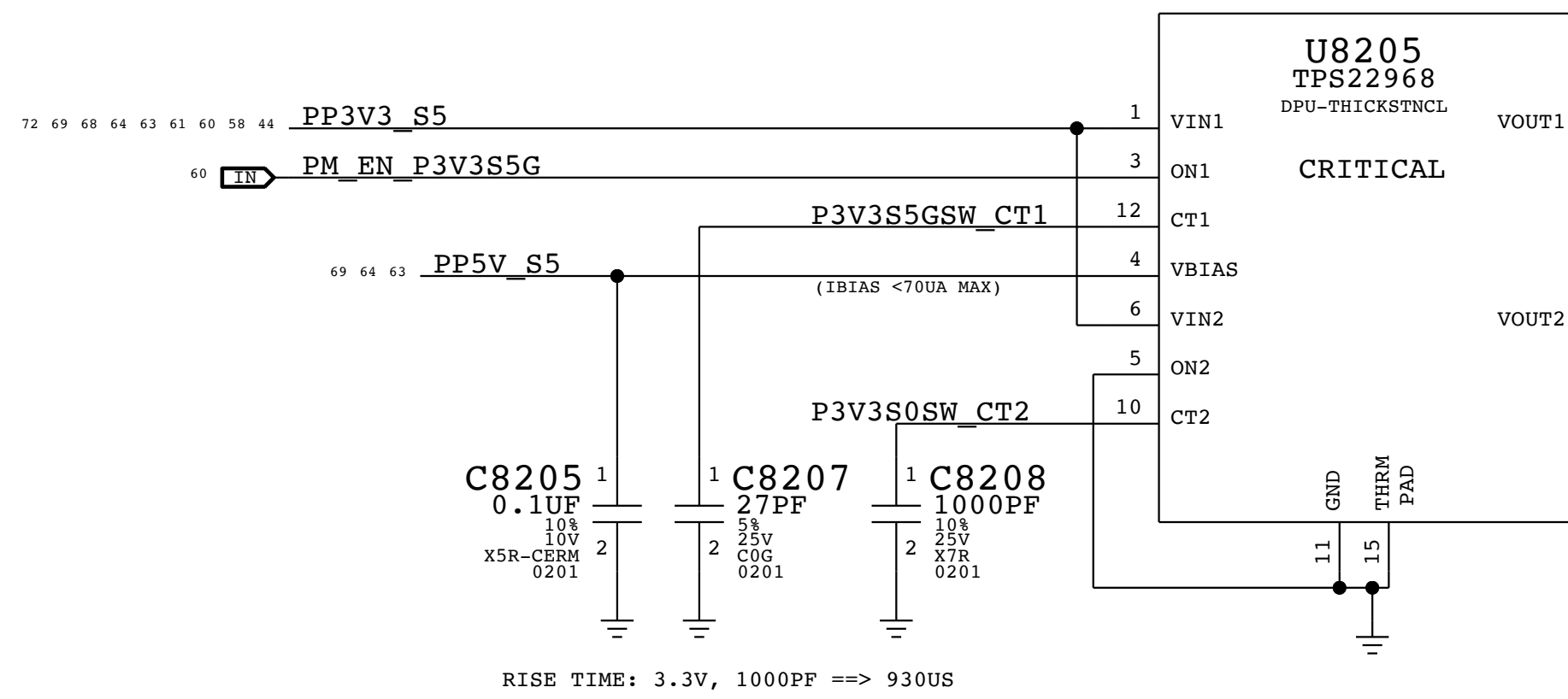
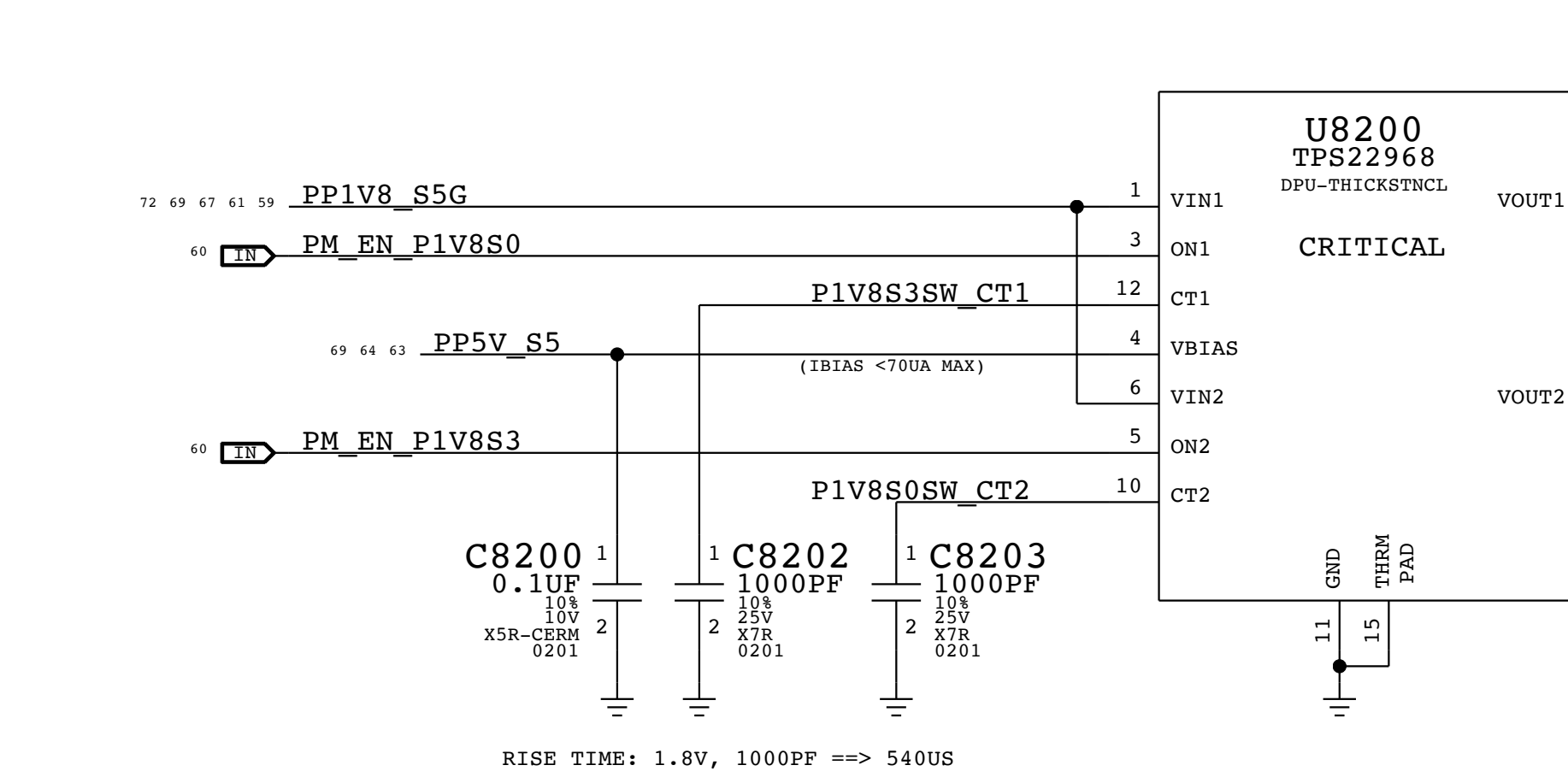
1V2 S0G SWITCH (VCCPLL\_OC)



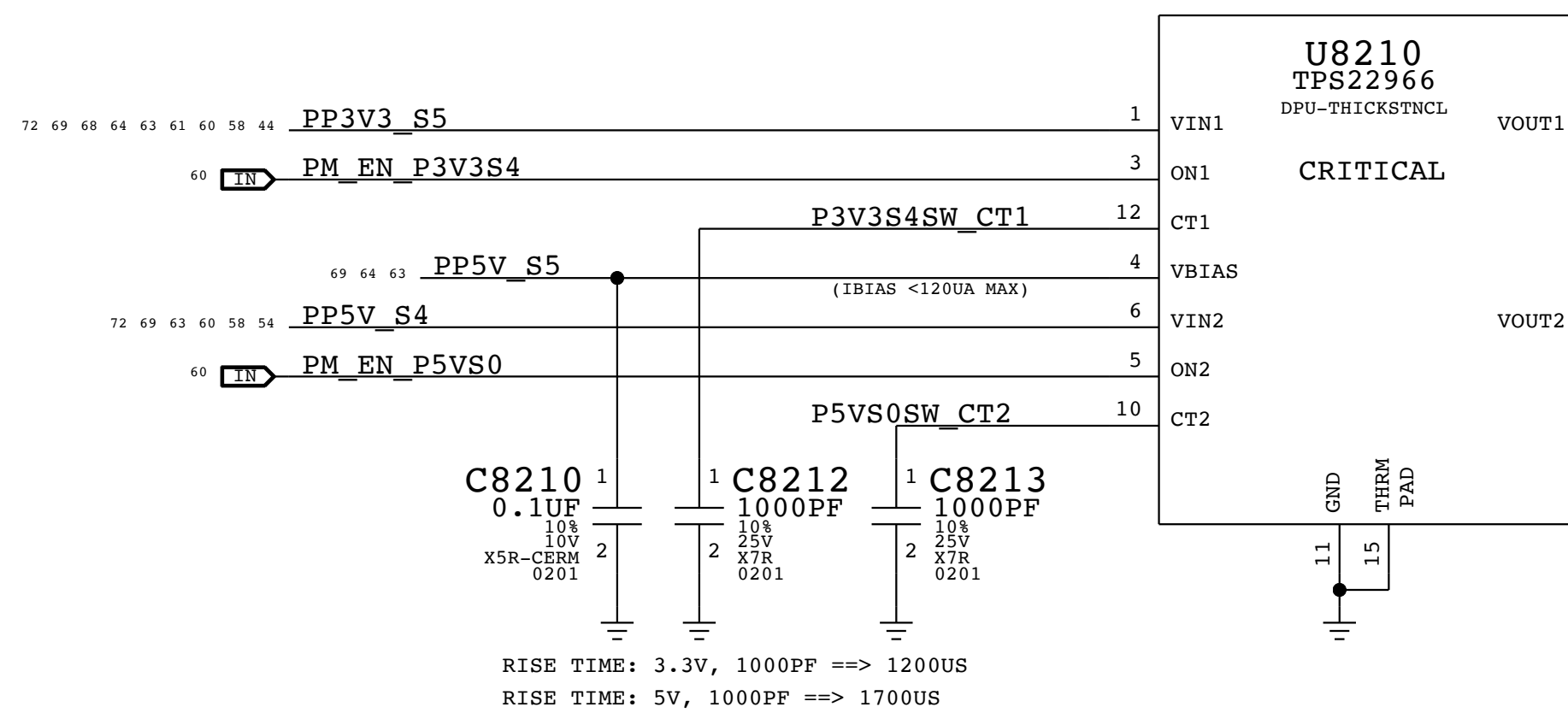
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Part	TPS22904
Type	Load Switch
R(on) @ 1.2V	135 MOHM TYP 185 MOHM MAX
Current	0.5A MAX
TON-TOTAL	20US MAX @ 1.2V



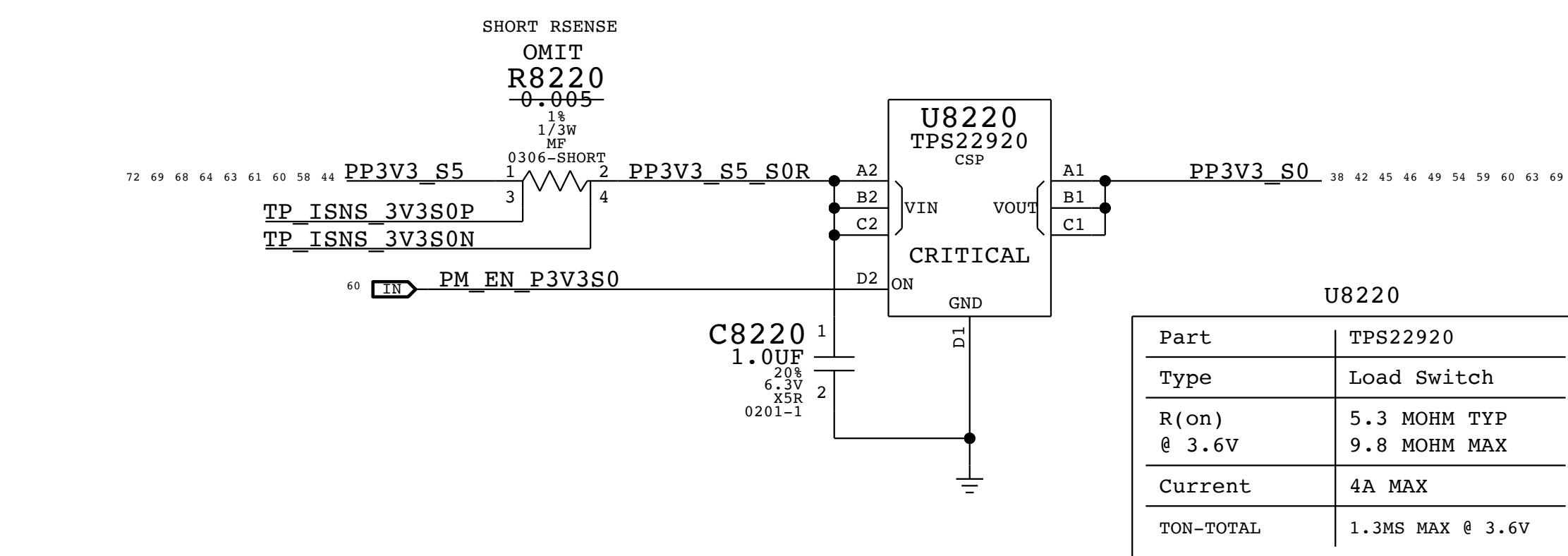
U8200	
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1MS MAX @ 1.8V



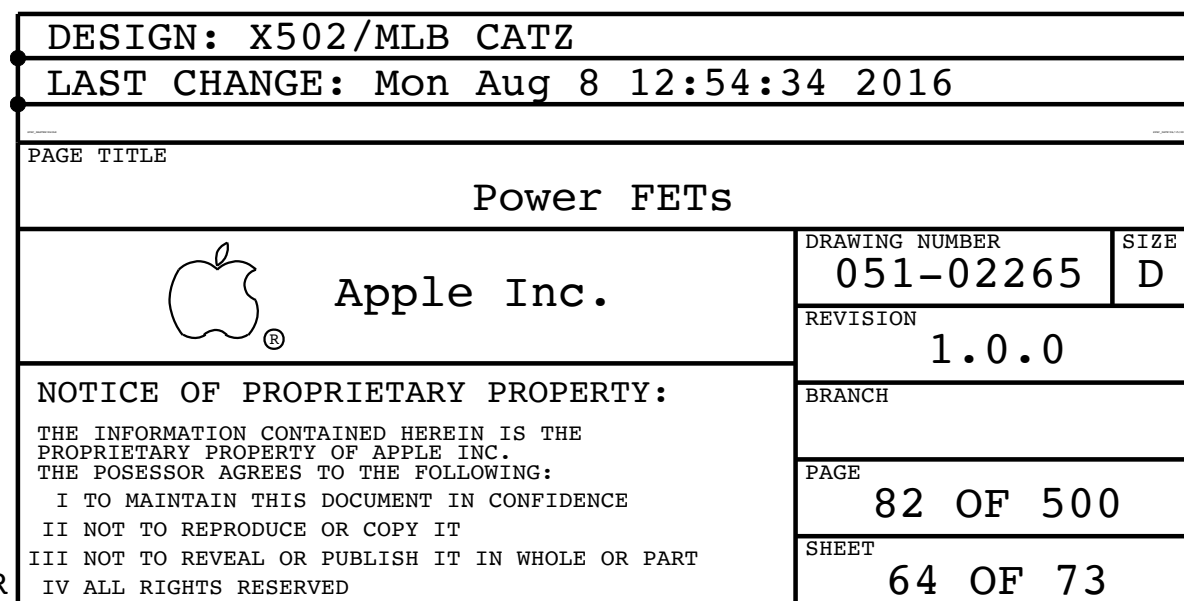
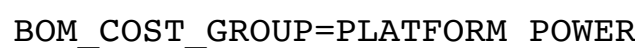
U8205	
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1.4MS MAX @ 3.3V



U8210	
Part	TPS22966
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	18 MOHM TYP 27 MOHM MAX
Current	6A MAX
TON-TOTAL	1.7MS MAX @ 3,3V 2.4MS MAX @ 5V



U8220	
Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.3 MOHM TYP 9.8 MOHM MAX
Current	4A MAX
TON-TOTAL	1.3MS MAX @ 3.6V



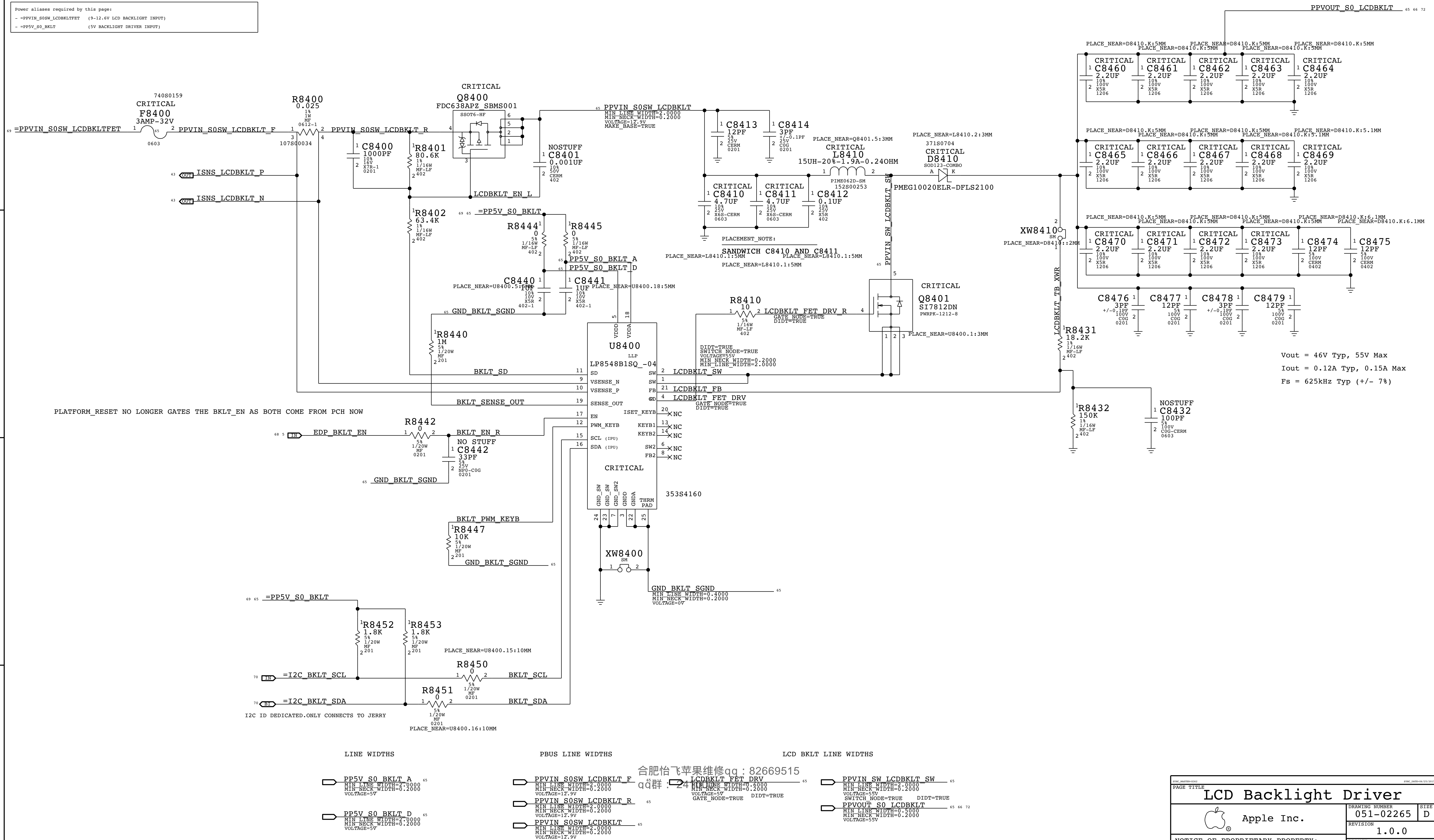


## Page Notes

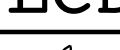
Power aliases required by this page:

- =PPVIN\_S0SW\_LCDBKLTFT (9-12.6V LCD BACKLIGHT INPUT)

```
- =PP5V_S0_BKLT      (5V BACKLIGHT DRIVER INPUT)
```



BOM\_COST\_GROUP=DISPLAY

PAGE TITLE		LCD Backlight Driver	
	Apple Inc.		
	DRAWING NUMBER	051-02265	SHEET D
	REVISION	1.0.0	
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		SHEET	65 OF 73



LCD PANEL INTERFACE (eDP) + Camera (MIPI)

LCD Panel HPD & AUX strapping

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		SHEET	
		85 OF 500	66 OF 73

BOM\_COST\_GROUP=DISPLAY

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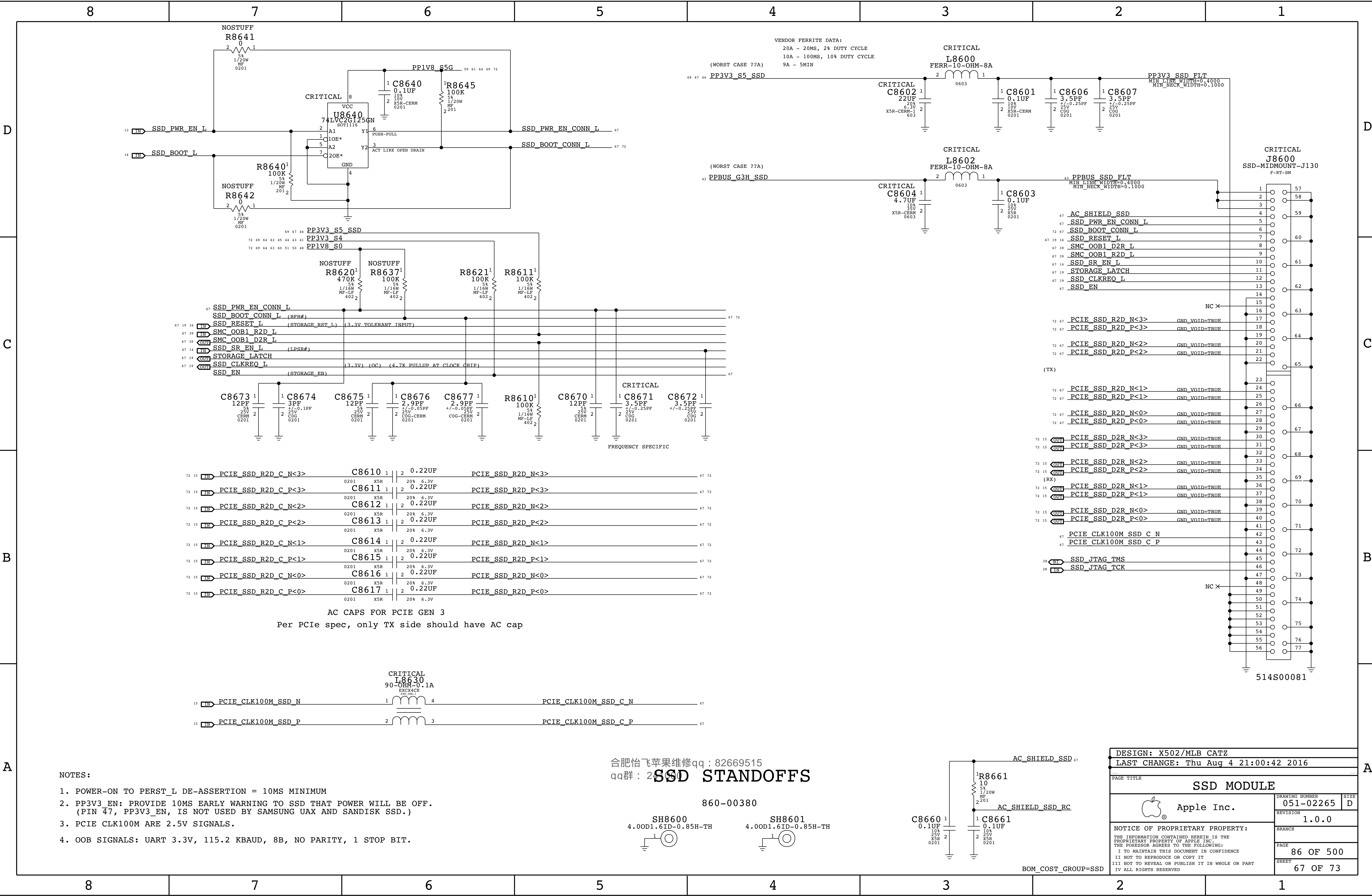
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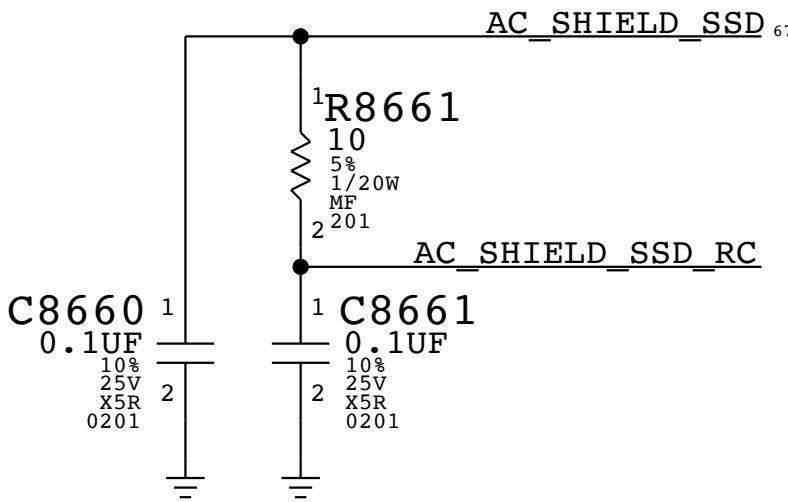
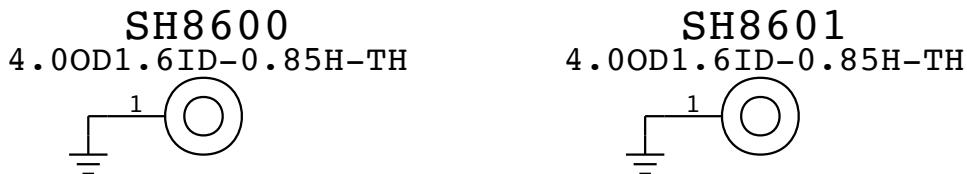


- NOTES:
- POWER-ON TO PERST\_L DE-ASSERTION = 10MS MINIMUM
  - PP3V3\_EN: PROVIDE 10MS EARLY WARNING TO SSD THAT POWER WILL BE OFF. (PIN 47, PP3V3\_EN, IS NOT USED BY SAMSUNG UAX AND SANDISK SSD.)
  - PCIe CLK100M ARE 2.5V SIGNALS.
  - OOB SIGNALS: UART 3.3V, 115.2 KBAUD, 8B, NO PARITY, 1 STOP BIT.

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qq群 : 245555555

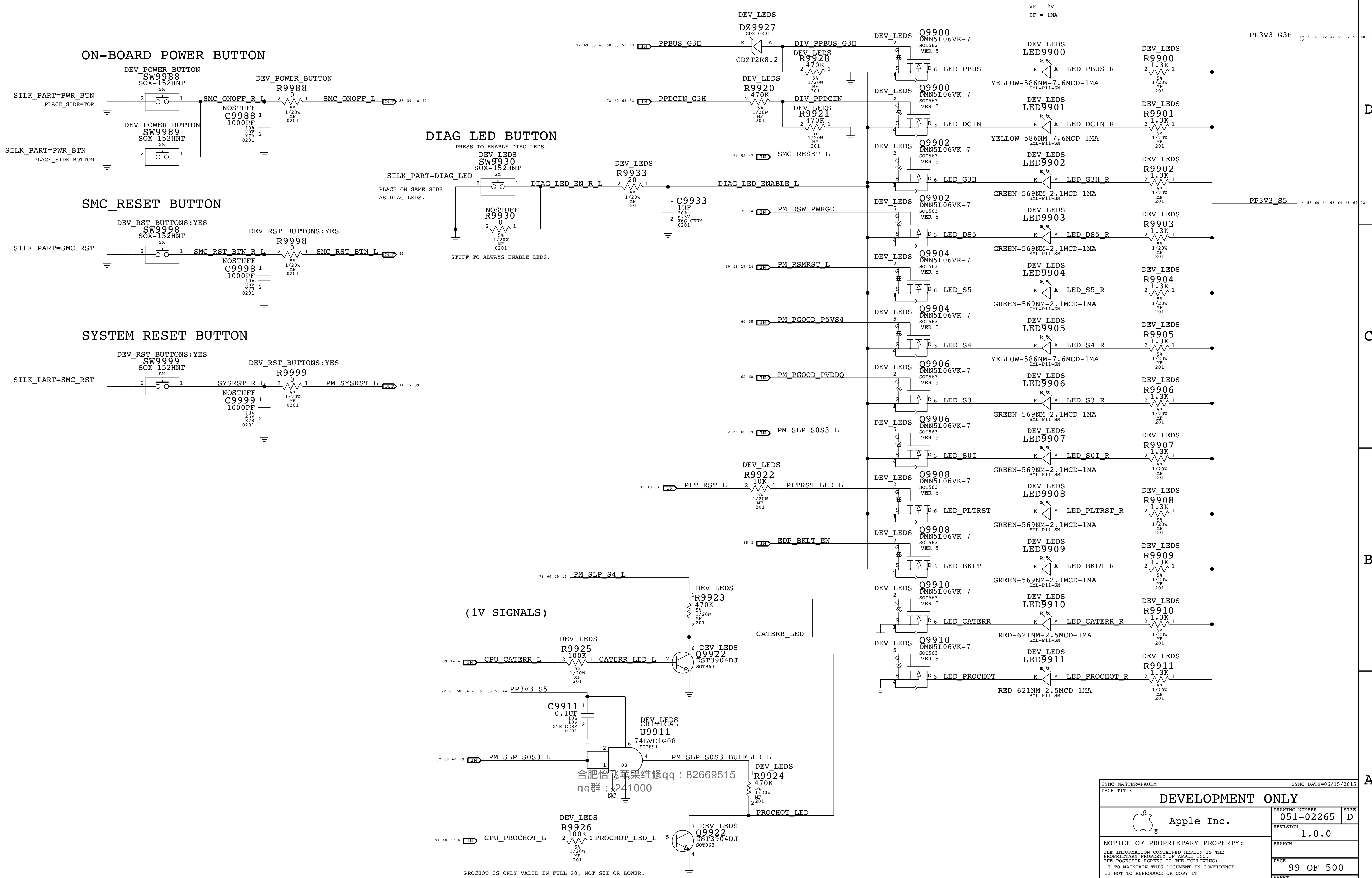
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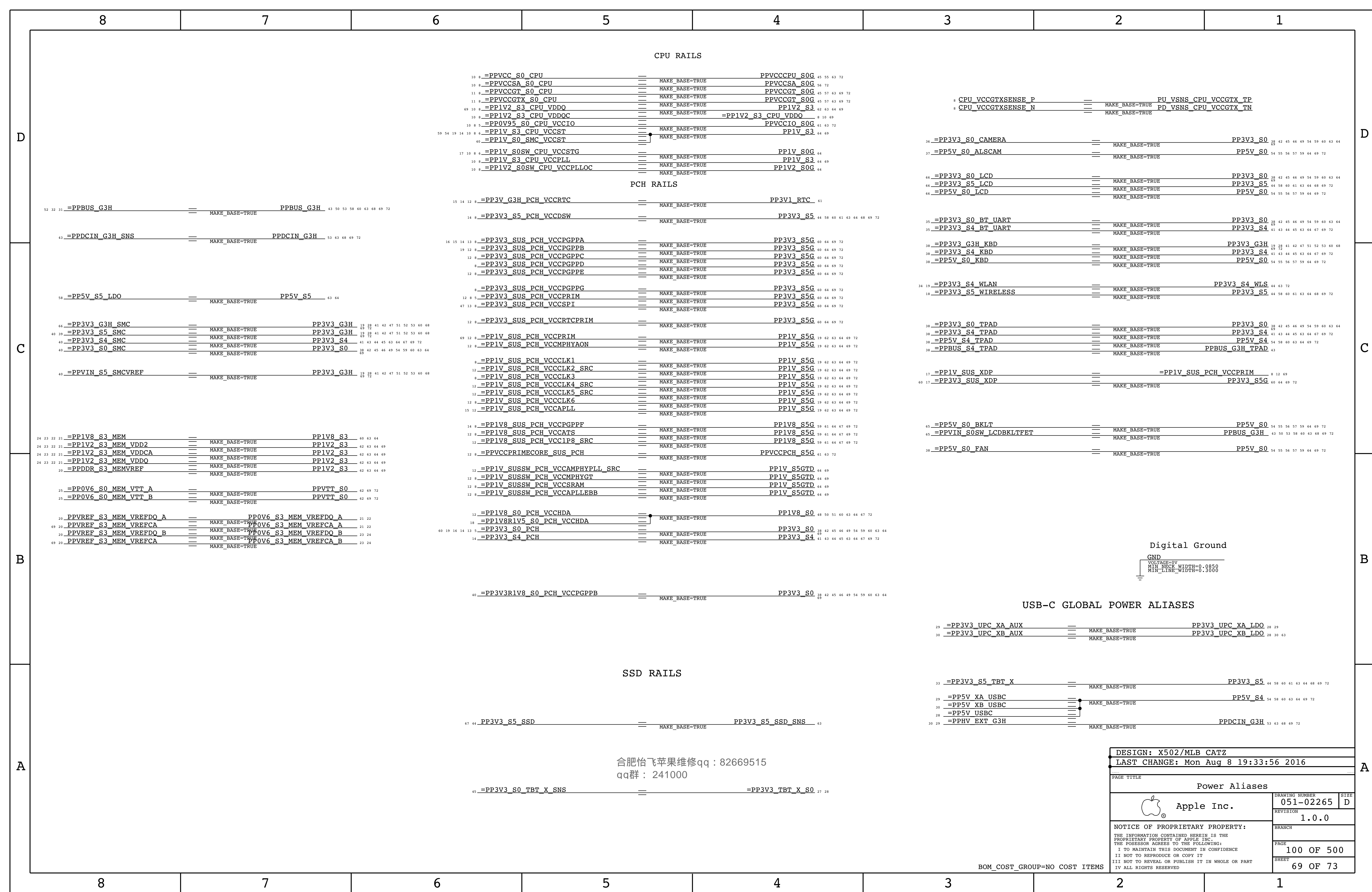
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BOM\_COST\_GROUP=SSD

DESIGN: X502/MLB CATZ		
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8		7		6		5		4		3		2		1												
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	MAKE_BASE							MAKE_BASE																		
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DESIGN: X502/MLB CATZ		
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Memory Signal Swaps		
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8	7	6	5	4	3	2	1
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C							C
B							B
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LAST SCHEMATIC PAGE.

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